TM 11-6625-1826-40

TECHNICAL MANUAL

GENERAL SUPPORT MAINTENANCE MANUAL

FOR

TEST SET, TERRAIN-CALIBRATION

INDICATOR AN/AAM-33

HEADQUARTERS, DEPARTMENT OF THE ARMY

W a r n i n g

DEATH or SERIOUS INJURY may result from HAZARDS in this equipment. PEAD and OBSERVE the following WARNINGS.

W A R N I N G

DEATH or SERIOUS INJURY may result from contact with 115-VAC, 400-Hz, 3-PHASE power existing within this equipment.

TM11-6625-1826-40
C2

CHANGE
No. 2

HEADQUARTERS,
DEPARTMENT OF THE **ARMY**
WASHINGTON, DC, 21 February ***1978***

General Support Maintenance Manual
TEST SET, TERRAIN-CALIBRATION INDICATOR AN/AAM-33
(NSN 6625-00-403-1070

TM 11-6625-1826-40, 20 October 1970, is changed as follows:
1. Title of manual is changed as shown above.
2. A vertical bar appears opposite changed material.
3. Remove and insert pages as indicated on the page list below:

	Insert
i	i/(ii blank
1-1	1-1/(1-2 blank)
2-1 and 2-2	2-1 and 2-2
2-9 and 2-10	2-9 and 2-10
3-1 through 3-19	3-1 through 3-19
FO-4 (fig. FO-3 ❷)	FO-4 (fig. FO-3 ❷)
FO-6 (fig. FO-5)	FO-6 (fig. FO-5)

4. File this change sheet in ***front*** of the manual for reference purposes.

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CHANGE No. 1

HEADQUARTERS
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General Support Maintenance Manual

TEST SET, TERRAIN-CALIBRATION INDICATOR AN/AAM-33

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Remove pages	Insert pages
1-1, 1-2	1-1, 1-2
2-7, 2-8	2-7, 2-8
3-1 through 3-20	3-1 through 3-19
FO-4 (figure FO-3 (2))	FO-4 (figure FO-3(2))

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GENERAL SUPPORT MAINTENANCE MANUAL
TEST SET, TERRAIN CALIBRATION INDICATOR AN/AAM-33
(NSN 6625-00-403-1070

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CHAPTER 1
INTRODUCTION

1-1. Scope of Manual

a. This manual contains functioning of equipment and general support maintenance for Test Set, Terrain-Calibration Indicator AN/AAM-33 (indicator test set). General support maintenance includes troubleshooting, and replacement, adjustment and alignment, repair, and general troubleshooting.

b. Operator and organizational maintenance procedures are contained in TM 11-6625-1826-12.

1-2. Indexes of Publications

a. Refer to the latest issue of DA Pam 310-4 to determine if there are new editions, changes, or additional publications pertaining to the equipment.

b. Refer to the latest issue *of* DA Pam 310-7 to determine whether there are modification work orders (MWO's) pertaining to the equipment.

NOTE

Applicable forms and records are covered in TM 11-6625-1826-12.

1-3. Reporting of Errors

The reporting of errors, omissions, and recommendations for improving this publication by the individual user is encouraged. Reports should be submitted on DA Form 2028 (Recommended Changes to Publications and Blank Forms) and forwarded direct to Commander, US Army Electronics Command, ATTN: DRSEL-MA-Q, Fort Monmouth, NJ 07703.

1-3.1. Reporting Equipment Improvement Recommendations (EIR)

EIR's will be prepared using DA Form 2407 (Maintenance Request). Instructions for preparing EIR's are provided in TM 38-750, the Army Maintenance Management System. EIR's should be mailed direct to Commander, US *Army* Electronics Command, ATTN: DRSEL-MA-Q, Fort Monmouth, NJ 07703. A reply will be furnished direct to you.

1-4. Reference Designations

Reference designations for major components of Test Set, Terrain-Calibration Indicator AN/AAM-33 are listed in TM 11-6625-1826-12.

CHAPTER 2

FUNCTIONING OF EQUIPMENT

Section I. BLOCK DIAGRAM FUNCTIONING

2-1. Overall Function

The indicator test set performs a bench test of either Terrain Display Indicator IP-970/AAS-24 (tdi), or Calibration Display Indicator IP-969/AAS-24 (cdi). The tdi is tested for brightness, contrast focus, interlace, resolution, linearity and centering. The cdi is tested for brightness and focus. Each unit is tested separately without disturbing Detecting Set, Infrared AN/AAS-24.

2-2. Block Diagram (fig. FO-2)

a. Ac Power Distribution. The 115-vac, 400-Hz, 3-phase ac power is applied through jack 1A1J2, through the filters (FL) and circuit breaker (CB2) to the contacts of standby relay 1A1K1. When standby relay 1A1K1 energizes a path is completed to the dc power supplies and to phase sensing relay 1A1K4 and to power transformer 1A1T1, where the ac is stepped up or down, applied to 1A1A5 through 1A1A7, and rectified and filtered to supply dc power required for operation of the indicator test set. The phase sensing relay K4 senses the 3-phase ac and if all phases are correct, operates to provide a path for +5 vdc to power control 1A1A4. When operate relay 1A1K2 operates, 115-vac, 400-Hz, 3-phase is applied to the unit under test.

b. Dc Power Distribution. The 28-vdc power is applied through 1A1J1, the filters, and CB1 to the power mode switch. Setting the power mode switch to STBY furnishes the 28 vdc to standby relay 1A1K1 causing it to operate and apply the 28 vdc through the restored contacts of operate relay 1A1K2 to light the STBY lamp. Setting the power mode switch to OPR operates operate relay 1A1K2, extinguishes the STBY lamp, lights the OPR lamp, and operates power relay 1A1K3 which furnishes +5 vdc, +150 vdc, –15 vdc, and +15 vdc to the unit under test and +150 vdc to miscellaneous circuits 1A1A3. With the power mode switch in either STBY or OPR, +5 and +15 vdc is applied to video generator 1A1A1, +15 and –15 vdc is applied to video processor 1A1A2, and +5, +15, and –15 vdc is applied to miscellaneous circuits 1A1A3.

c. Test Points. External signals from the unit under test are applied to the indicator test set and are routed to the TEST POINTS section on the control panel by the TEST POINTS switch 1A1S7. Power supplies are also routed to this switch for monitoring.

d. Dc Power Supplies.

(1) The +15, –15, and +150-vdc power supply outputs are applied to heatsink 1A1A9 to accomplish heat dissipation. The output voltages of heatsink 1A1A9 provide operating power to the printed circuit boards and the unit under test. Each power supply also furnishes its output to power control 1A1A4 for monitoring.

(2) The +5-vdc power supply 1A1A7 does not utilize the heatsink 1A1A9 for heat dissipation but does have an input of +15 vdc from heatsink 1A1A9. The output of the +5-vdc power supply 1A1A7 is applied to the phase sensing relay 1A1K4. If the ac phase sequence is correct, relay 1A1K4 operates and the +5-vdc power supply output is applied to power control 1A1A4 for monitoring.

e. Power Control 1A1A4. Power control 1A1A4 monitors each of the dc power supplies. If any of the monitored inputs varies, power control 1A1A4 removes operating power from the indicator test set and the unit under test and causes the FAIL lamp to light by removing the ground from relays 1A1K2, 1A1K3, and the OPR lamp. If the indicator test set is in the operate mode when a fail condition occurs, the indicator test set goes to standby, the STBY lamp lights and the OPR lamp is extinguished. To reactivate the indicator test set, the power mode switch is set to RESET and released. The power mode switch is spring loaded, so it returns to the OPR position. If all inputs to power control 1A1A4 are correct, the indicator test set remains

in the operate mode as indicated by the lighted OPR lamp The phase sensing relay lAlK4 operates as long as the input power continues to have the proper phase rotation. If the input power fails in this respect, the phase sensing relay 1A1K4 restores to remove the +5-vdc input power to power control lAlK4. This condition causes the FAIL lamp to light, the STBY lamp to light and the OPR lamp to extinguish. The indicator test set is reactivated by setting the power mode switch to RESET.

f. Video Generator 1A1A1. Video generator 1A1A1 generates output signal frequencies to test the tdi ***or*** cdi. Its outputs are vertical sync to test point 20, 50 Hz, 100 Hz, and 25 kHz to miscellaneous circuits 1A1A3 and video to video processor 1A1A2.

g. Video Processor 1A1A2. Video processor 1A1A2 applies video to the tdi and one of four selected signals, controlled by the CALIBRATION INDICATOR INPUT switch, to the cdi.

h. Miscellaneous Circuits 1A1A3. Miscellaneous circuits 1A1A3 receives 25 kHz, 100 Hz, and 50 Hz from video generator 1A1A1 and generates reticle ramp, tdi horizontal sync, read vertical sync, brightness, and tdi step to the tdi and horizontal sync and video gate to the cdi.

Section II. CIRCUIT FUNCTIONING

2-3. Equipment Interconnection (fig. 2-l)

A complete indicator test set is formed by connecting the equipment as shown in figure 2-l.

2-4. Circuit Functioning (fig. F0-3)

a. AC Power Distribution

(1) The 115-vac, 400-Hz, 3-phase power enters the indicator test set through lAlJ2-A, B, C, and D. This input is applied to filter 1A1A10. The 115-vac, 400-Hz, 3-phase output of filter lAlAl0 is applied through CB2 to standby relay 1A1K1-A2, B2, and C2 and to phase sensing relay 1A1K4-0A, 0B, and 0C. The neutral line is connected to a ground terminal. Phase sensing relay K4 monitors the phase rotation of the input ac power and operates to provide a path from 1A1K4-A2 to 1A1K4-A1 for the +5-vdc power supply to be monitored by power control 1A1A4. A missing phase or improper phase rotation causes K4 to restore and remove the +5 vdc from power control 1A1A&14.

(2) Setting the power mode switch to STBY (standby) causes the standby relay 1A1K1 to operate applying phase A through contacts Al and A2; phase B through contacts B1 and B2; and phase C through contacts Cl and C2; to the pow-

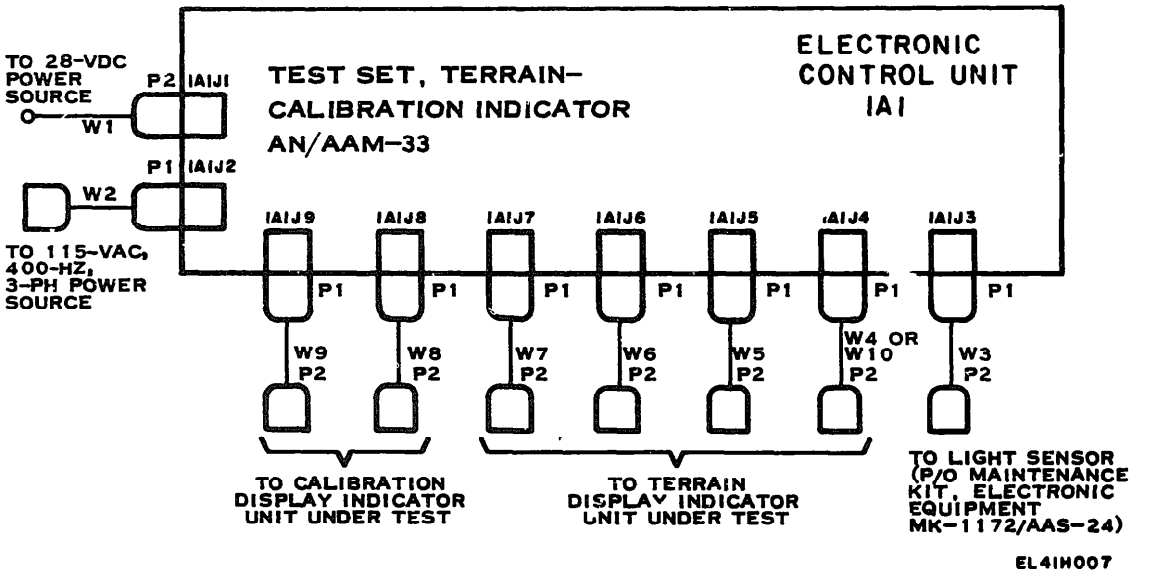


Figure 2-1. Interconnecting diagram.

er transformer 1A1T1, pins 1, 2, and 3, respectively. This power is also applied to the oper contacts of operate relay 1A1K2–A2, B2, and C2. The secondary of 1A1T1 develops 10.4-vac, 400-Hz, 3-phase power for the +5-vdc power supply 1A1A7; 22 vac, 400-Hz, 3-phase power for the –15-vdc power supply ; 22-vac, 400-Hz, 3-phase power for the +15-vdc power supply; and 232-vac, 400-Hz, 3-phase power for the +150/+250-vdc power supply.

(3) Setting the power mode switch to OPR (operate) causes the power supply relay 1A1K2 to operate and furnish power to 1A1J9–A, B, and C and 1A1J5–A, B, and C through contacts A1 and A2; B1 and B2; and C1 and C2, respectively. This output is applied to the tdi through 1A1J5 and the cdi through 1A1J9.

b. De Power Distribution.

(1) The 28-vdc power enters the indicator test set through 1A1J1–A and B. The output 28 vdc from filter 1A1A10 is applied through CB1 and CR1.

(2) Setting the power mode switch 1A1S4 to STBY applies 28 vdc through 1A1S4–C1 to contact 1A1K1–X1, causing it to operate; 28-vdc power is then applied to 1A1S4A–C2 wiper. The K1 closed contacts D1 and D2 allow power to be applied to STBY lamp DS2–2 through 1A1K2–D2 and D3 causing the STBY lamp to light. 28-vdc FAIL power is also applied to power control 1A1A4–4.

(3) Setting the power mode switch to OPR causes latch out 28-vdc power to be applied to power control 1A1A4–9. This latch out power enables the power control 1A1A4 to maintain a steady FAIL indication, even under fluctuating power conditions, until the power mode switch is set to RESET. Contact wiper 1A1S4A–C2 furnishes 28 vdc to contact 7 and operates operate relay 1A1K2. The 1A1K2 open contacts D2 and D3 cause STBY lamp DS2 to extinguish, and the closed contacts D1 and D2 cause OPR lamp DS3 to light and power relay 1A1K3 to operate.

(4) The +15-vdc power supply 1A1A5 +27-vdc unregulated output is applied to heatsink 1A1A9J11, pin 14; +15 vdc for regulation is applied to 1A1A9J11, pin 11. Heatsink 1A1A9 +15-vdc output is sampled and returned to 1A1A5–1 to control the regulated output. The +15-vdc power utilized in the indicator test set is furnished from 1A1A9J11, pins 1, 2, 3, and 4.

(5) The –15-vdc power supply 1A1A6 is the same as the +15-vdc power supply except for application. The unregulated output is +12 vdc at 1A1A6–4 and is applied 1A1A9J11, pin 21. The regulator drive is +1.5 vdc and is applied to 1A1A9J11, pin 22. The –15 vdc is developed at 1A1A6–13 and 6 and applied to the printed circuit boards for power. Ground return is developed at 1A1A9J11, pin 23.

(6) The integrated circuit power supply 1A1A7 has +15 vdc applied at 1A1A7–23 from 1A1A9J11, pin 2, and –15 vdc at 1A1A7–2 from the –15-vdc supply. These inputs provide power for an amplifier and a voltage divider network. The +5 vdc is developed at 1A1A7–1 and 3 and applied to the printed circuit boards for power. Ground return is 1A1A7–12 and 13.

(7) The +150/+250-vdc power supply 1A1A8 provides +150 vdc at 1A1A8–18 and 16. The 150 vdc is applied to the power control for monitoring and to miscellaneous circuits 1A1A8 in the operate mode. The reference resistors 1A1R6, 1A1R7, 1A1R8, 1A1R9, and 1A1R10 determine the voltages at pins 1A1A8–1, 3, 5, 12, and 10 and the output of the power supply.

(8) Heatsink 1A1A9 (fig. 2–2) is used to dissipate excess heat for the +15 vdc, –15 vdc, and +150-vdc power supplies. The outputs are +15 vdc at 1A1A9J11, pins 1, 2, 3, and 4 and +150 vdc at 1A1A9J11, pins 18 and 16. The –15-vdc power supply does not develop its output through heatsink 1A1A9, but establishes a ground reference at 1A1A9–23.

(9) The 28-vdc return for relays 1A1K2 and 1A1K3 originates at 1A1A4–6. As long as ac and dc voltages are correct, the 28-vdc return allows relays K2 and K3 to operate and provide a path for supplying voltages to the unit under test. The 28-vdc return path can be traced as follows: From 1A1A4–6 to 1A1A4–11, out of the indicator test set at 1A1J5–J and 1A1J9–s, back into the indicator test set at 1A1J5–H and 1A1J9–t, and then to K2–X2 and K3–X2. If 1A1A4 senses an incorrect voltage, the 28-vdc return is disrupted. Without the 28-vdc return, K2 and K3 restore to prevent ac and dc power from being applied to the unit under test. The STBY lamp DS2 will light and the OPR lamp DS3 will extinguish.

c. Video Generator 1A1A1. Video generator 1A1A1 develops output signals of 50 Hz, 100 Hz, 25 kHz, vertical sync and video. The 25 kHz at 1A1A1–2, the 100 Hz at 1A1A1–6 and vertical sync at 1A1A1–19 are always present when the indicator test set is being operated. The 50 Hz at 1A1A1–23 is activated by the 50 Hz command input. The video at 1A1A1–17 is a result of one or more command input signals which cause

various outputs to the unit under test. The VIDEO SELECT switch 1A1S6, PATTERN switch 1A1S1, FIELD OF VIEW switch and CAL IND CONTRGLS INPUT switch 1A1S5 select the path for the command input signals. A logic 1 output signal is always present at 1A1A1–21. This signal is applied to VIDEO SELECT switch 1A1S6 and to FIELD OF VIEW switch 1A1S3. Positioning VIDEO SELECT switch to TD or CI applies the logic 1 signal to PATTERN switch 1A1S1 or INPUT switch 1A1S5. Setting PATTERN switch 1A1S1 to each of its 5 positions of the INPUT to each of its 4 positions stimulates video generator 1A1A1 to apply the output at 1A1A1–17 as a result of the command inputs. The FIELD OF VIEW switch 1A1S3 applies the logic 1 command signal to the PATTERN switch 1A1S1 for application to 1A1A1–14 only when PATTERN switch 1A1S1 is in position 3.

d. Video Processor 1A1A2. Video processor 1A1A2 receives video from video generator 1A1A1 and applies it to the tdi and switches it to the cdi. The tdi output is always present at 1A1A2–3 as long as there is an input at 1A1A2–22. The cdi output is dependent on the INPUT switch 1A1S5 to select video 1, 2, 3, or 4. The INPUT switch 1A1S5 applies the selected input to 1A1A2–1 or 8, or both 1 and 8. This input determines whether video is present at pins 2, 6, 10, or 12.

e. Miscellaneous Circuits 1A1A3. Miscellaneous circuits 1A1A3 receives inputs of 25 kHz, 100 Hz, and 50 Hz and develops outputs to apply to tdi or cdi. The 25 kHz input causes reticle ramp and tdi horizontal to be sent to the tdi and causes calibration indicator horizontal sync to be set to the cdi. The 100 Hz input causes the video gate signal to be sent to the cdi. The 50 Hz input causes both read vertical sync and tdi step signals to be applied to the tdi. The brightness voltage output at 1A1J4–2 is developed from the +150-vdc input and adjusted by the external BRIGHTNESS potentiometer 1A1R3.

f. TEST POINTS Switch 1A1S7.

(1) TEST POINTS switch 1A1S7 is used to transfer internal indicator test set signals to control panel 1A1 panel mounted test points for monitoring. TEST POINTS switch 1A1S7 is an 8-contact, 5-deck, rotary switch. The wiper for each deck is connected to panel mounted jacks (test points).

(2) Deck A wiper is connected to test point 1. The contacts of this deck, the signals monitored at each contact, and the origin of the signal monitored are shown in table 2–1.

(3) Deck B wiper is connected to test point 2. The contacts of this deck, the signals monitored at each contact and the origin of the signals monitored are shown in table 2–2.

(4) Deck C wiper is connected to test point 3. The contacts of this deck, the signals monitored at each contact and the origin of the signals monitored are shown in table 2–3.

Table 2-1. TEST POINTS Switch 1A1S7, Deck A

Contact	Signal	Origin
1	+150 vdc	1A1A8–16
2	+ 40 vdc	1A1J7–H
3	– 25 vdc	1A1J7–J
4	+ 30 vdc	1A1J7–K
5	+ 80 vdc	1A1J7–L
6	High voltage sample	1A1J6–H
7	Tdi fail	1A1J5–K
8	Horizontal deflection drive	1A1J6–C

Table 2-2. TEST POINTS Switch 1A1S7, Deck B

Contact	Signal	Origin
1	+15 vdc	1A1A5–2
2	Contrast control	1A1R4–2
3	Brightness (10 to 80 vdc)	1A1R3–2
4	Reticle intensity	1A1R2–2
5	Negative vertical deflection	1A1J6–E
6	Positive vertical deflection	1A1J6–F
7	Selected slew voltage	1A1J5–AA
8	Gain 3 control	1A1J4–S

(5) Deck D wiper is connected to test point 4. The contacts of this deck, the signals monitored at each contact and the origin of the signals monitored are shown in table 2–4.

(6) Deck E wiper is connected to test point SCOPE. The contacts of this deck, the signals monitored at each contact and the origin of the signals monitored are shown in table 2–5.

Table 2-3. TEST POINTS Switch 1A1S7, Deck C

Contact	Signal	Origin
1	–15 vdc	1A1A6–13
2	+12 vdc	1A1J9–Z
3	– 6 vdc	1A1J9–a
4	+300 vdc	1A1J9–b
5	+150 vdc	1A1J9–c
6	1.5 k vdc	1A1J9–u
7	Slew voltage output	1A1J5–y
8	Gain 2 control	1A1J4–R

Table 2-4. TEST POINTS Switch 1A1S7, Deck D

Contact	Signal	Origin
1	+5 vdc	1A1A7–1
2	No connection	–
3	Manual v/h	1A1J4–d
4	Tdi sweep	1A1J5–s
5	–1.5 k vdc	1A1J9–V
6	Blanking	1A1J9–Y
7	0° slew	1A1J5–z
8	Hot target mode	1A1J4–G

Table 2-4. TEST POINTS Switch 1A1S7, Deck E

Contact	Signal	Origin
1	Video intensity	1A1R1-Z
2	Reticle ramp	1A1A3-13
3	No connection	-
4	Tdi step	1A1A3-2

Table 2-5. TEST POINTS Switch 1A1S7, Deck E--continued

Contact	Signal	Origin
5	Read vertical sync	1A1A3-5
6	Video gate	1A1A3-1
7	Light sensor output	1A1J3-D
8	Horizontal deflection sample	1A1J6-K

Section III. PRINTED CIRCUIT BOARD FUNCTIONING

2-5. Video Generator, 1A1A1 (fig. FO-4)

The video generator consists of a 10-mHz oscillator, frequency dividers and logic gates.

a. The 10-mHz oscillator is composed of transistor Q1, capacitors C3 and C4, resistors R1, R2, R3, and crystal Y1. The output is applied to pins 12 and 13 of AND logic ic 1A1A1Z11A. This amplifier-buffer applies its output to 1A1A1Z11D-2, 1A1A1Z8B-1 and 1A1A1Z12-1.

b. Frequency dividers divide the 10-mHz oscillator output as follows:

(1) Network Z12 divides by 4 and by 2 yielding a 2.5-mHz signal at Z12-9 and a 5-mHz signal at Z12-5. The 5-mHz signal at Z12-5 is applied to Z12-12 as an input to obtain the 2.5-mHz signal at Z12-9. The 2.5-mHz signal is applied to Z9-14, Z13-3, Z8B-2 and the 5-mHz signal is applied to Z13-2.

(2) The 2.5-mHz signal is divided by 10 and by 2 by network Z9. The 1.25 mHz is applied to Z13-6, Z8B-4 and Z9-1 to obtain the 250-kHz signal. The 250-kHz signal at Z9-11 is applied to gate Z13-12, gate Z5-4, and to divider Z10-1.

(3) Network Z10 divides the input by 5 and by 10. The 25-kHz signal at Z10-12 is applied to 1A1A1J1-2 as 25-kHz output. The 50-kHz signal at Z10-11 is applied to divider Z7A-14 and Z10-14 to obtain the 25 kHz at Z10-12.

(4) Divider network Z7A divides the input by 2. The 25-kHz output is applied to Z2-12 and divider network Z3A-14.

(5) Divider network Z3A divides the input by 2. The 12.5-kHz output is applied to Z8A-12, to Z2-4, to Z5-1, and to divider Z3B-1.

(6) Divider Z3B is a divide by 5 network. The 2500-Hz output is applied to Z8A-10, to Z2-5, 6, 9, and to divider Z7B.

(7) Divider Z7B is a divide by 5 network. The 500-Hz output is applied to Z3-13, to X2-1, and to divider Z6.

(8) Divider Z6 divides the input by 10 and by 5. The divide by 10 output of 50 Hz is applied to Z1C-12, to Z2-3, to Z1A-4, and to the base of Q2. The collector of Q2 is connected to P1-19 to become the vertical sync output. The divide by 5, 100-Hz output is applied to P1-6 as 100 Hz. The input at Z6-14 obtains the 50 Hz at Z10-12.

c. For the logic portion of the video generator, notice that all the gates are 'NAND' gates. The logic code is, any low input gives a high output, all high inputs are necessary to give a low output. A logic (high) is the output at 1A1A1-21. This signal is applied to VIDEO SELECT 1A1S6, where it is switched to either CAL IND CONTROLS INPUT switch 1A1S5, or PATTERN switch 1A1S1. One other path for this signal is through FIELD OF VIEW switch 1A1S3 to PATTERN switch 1A1S1. The logic 1 (high) passes through the contacts of these switches and is reapplied to video generator 1A1A1 as the command signals; 12.5-kHz command, 1A1A1-16; 250-kHz command, 1A1A1-15; 50-Hz command, 1A1A1-14; interlace command, 1A1A1-4; contrast command, 1A1A1-12; linearity command, 1A1A1-10; reticle command, 1A1A1-1; resolution command, 1A1A1-20; and 10-mHz command, 1A1A1-22 to enable the NAND gates. The frequencies generated by the dividers are already present at the gates and pass through to 1A1A1-17 as the output video.

(1) The 50-Hz command is applied to P1-14 and Z1A-5. This high input to Z1A-5 results in Z1A applying a low to the base of Q3. The input at Z1A-4 is changing at a 50-Hz rate causing gating at a 50-Hz rate. The collector of Q3 changes to a high at this rate and provides a 50-Hz output at P1-23.

(2) The 12.5-kHz command at P1-16 is applied to Z5-2. The 12.5 kHz gates Z5 which already has 12.5 kHz on Z5-1. Thus a 12.5-kHz output is applied to Z4-11. Each negative pulse causes video output at P1-17.

(3) The 250-kHz command is very similar to the 12.5-kHz command. The 250-kHz command input at P1-15 is applied to Z5-5 and the output of Z5 is applied to Z4-4, 5, and 10 to develop the 250-kHz output at P1-17.

(4) The 10-mHz command at P1-22 is applied to Z11D-1 and the 10-mHz output is applied to Z4-2, 3, 13 to provide 10-mHz at P1-17.

(5) The contrast command at P1–12 is applied to Z1C–13. The 50-Hz output is applied to Z5A–12. The low pulses generate the output which is applied to Z5B–9, 10 and this output to Z4–6 for video output at P1–17.

(6) The resolution command at P1–20 is applied to Z8B–5. The combination of frequencies at Z8B–4, 1, and 2 cause low pulses to be applied to Z11C–9 and an output to Z11D–4. 5, and an output to Z4–12. This generates the output at Z4–8 to P1–17.

(7) The reticle command input at P1–1 is applied to Z13–11. The combination of frequencies at Z13–2, 3, 6, and 12 gate Z13 to give low pulses applied to Z11C–10. The video output is to Z11D, to Z4 and to P1–17.

(8) The linearity command input at P1–10 is applied to gate Z8A–9. The combination of frequencies present at Z8A–10, 12, and 13 then pass through to Z5A–13 to Z5B and to Z4. The output of Z4 is to P1–17 as the video signal.

(9) The interlace command at P1–4 is applied to Z2–11 to generate low gates at Z1B and a reset command to Z6–3, Z3A–3, and Z7A–3. This reset causes the 50Hz, vertical sync output to be triggered 20μ seconds sooner to cause the roll on the tdi.

d. The video output from all gates are applied to 1A1A1Z4 to 1A1A1–17 as the output to video processor 1A1A2.

2-6. Video Processor, 1A1A2 (fig. FO-5)

The video processor accepts the video signal from video generator 1A1A1, adjust the level according to the setting of VIDEO INTENSITY potentiometer 1A1R1, and furnishes a video output to the tdi or cdi unit under test. The video input from video generator 1A1A1 is applied to 1A1A2–22. Unijunction 1A1A2Q1 is biased by the VIDEO INTENSITY input at 1A1A2–23 which sets the signal level input to 1A1A2Z1. Push-pull power amplifier, Q2 and Q3, amplifies the signal before application to the tdi or cdi unit under test. The output to the tdi is at 1A1A2–3. The output to the cdi depends upon the CAL IND 1A1S5 switch position which selectively operates or restores 1A1A2K1 and 1A1A2K2. With the INPUT switch 1A1S5 in position 1, no ground is furnished to 1A1A2–1 or 8. Neither 1A1A2K1 nor 1A1A2K2 operate and the signal output is through the restored contacts of 1A1A2K1–B2 and B3 and 1A1A2K2–B2 and B3 to 1A1A2–12 as video 4. Set the INPUT switch to 2 and a ground is furnished from TB1–1, through 1A1S5–6 and 1A1A2–1 to 1A1A2K1–X2. The signal path is now through the closed contacts 1A1A2K1–B2 and B1 to restored contacts 1A1A2K2–A2 and A3 to 1A1A2–6 as video 2. When the INPUT switch is set to 3, a ground is applied to 1A1A2–1 and 8 to operate 1A1A2K1 and 1A1A2K2. This provides a signal path through the closed contacts of 1A1A2K1–B2 and B1 and closed contacts of 1A1A2K2–A2 and A1 to 1A1A2–2 for video 3. Set the INPUT switch to 4 and ground is applied to 1A1A2–8 to operate 1A1A2K2. The signal path is now through the restored contacts of 1A1A2K1–B2 and B3 to the closed contacts of 1A1A2K2–B2 and B1 to 1A1A2–10 for video 3.

2-7. Miscellaneous Circuits, 1A1A3 (fig. FO-6)

The miscellaneous circuits board consists of four separate circuits on one printed circuit board. The 25-kHz signal from video generator 1A1A1 enters the miscellaneous circuit board at 1A1A3–18. The signal triggers the monostable multivibrator consisting of 1A1A3Q3 and 1A1A3Q8. The output is amplified by 1A1A3Q13, Q16, Q19, and Q20. The tdi horizontal sync from the collector of Q19 is applied to 1A1A3–17. The calibration indicator horizontal sync from the collector of 1A1A3Q20 is applied to 1A1A3–16. The input to the reticle ramp circuit from the collector of 1A1A3Q16 is applied to the base of amplifier 1A1A3Q1. This reticle ramp input signal triggers the one-shot multivibrator composed of 1A1A3Q5 and Q7. This output is integrated by 1A1A3R35, 1A1A3C19, 1A1A3Q11, and 1A1A3Q12. The sweep is then amplified by 1A1A3Q15 and Q17, buffered by 1A1A3Q21 and power amplified by 1A1A3Q22 and Q23. The output is applied to 1A1A3–19 as reticle ramp. The 100 kHz from video generator 1A1A1 enters at 1A1A3–3. This input triggers the monostable multivibrator composed of 1A1A3Q4 and 1A1A3Q9. The output is amplified by 1A1A3Q14 and 1A1A3Q18 and applied to 1A1A3 pin 1 as video gate. The 50-Hz input from video generator 1A1A1 enters 1A1A3–6 and is applied to 1A1A3–8 as read vertical sync. The 50 Hz is also applied in parallel to 1A1A3Q6 and then to 1A1A3Q10. Both these transistors amplify the signal and apply it to 1A1A3–2 as tdi step. Brightness voltage is obtained by inserting 150 vdc at 1A1A3–12 through 1A1A3R11 to 1A1A3–14. BRIGHTNESS potentiometer 1A1R3 is connected externally with a return through 1A1A3–10, 1A1A3R55, and 1A1A3–9 to dc return.

2-8. Power Control, 1A1A4 (fig. FO-7)

The outputs of the +l56-vdc, +15-vdc, +5-vdc, and -15vdc regulated power supplies are applied to 1A1A4 P1-18, P1-16, P1-14, and P1-17 as sense voltages. If any of the four voltages sensed by the power control circuit exceeds the overvoltage or undervoltage limits, the dc return to the tdi unit or cdi unit under test and relays **1A1K2 and 1A1K3 is removed, removing power** from the unit under test. The four sense voltages are applied to four voltage dividers, **consisting of R4 through R11, which reduce each of** the applied voltages to three volts. The divided voltage from the -15-vdc power supply is inverted by unity-gain amplifier Z1. The four +3-vdc levels are applied through R12, R13, R14, and R20 to the level detectors as an **OR function and deviations in any one of the sensed** voltages will appear at C4. The OR function is applied to noninverting input Z2-3 and to inverting input **Z3-2.** A reference voltage is developed by resistor Rl and zener diodes **CR1 and** CR2. The reference level for overvoltage detector Z2 is established by potentiometer R21; the reference level for undervoltage detector **Z3 is es**tablished by R19. If the OR function input is either higher than the overvoltage reference level or lower than the undervoltage reference level, the output at **Z2-6** or **Z3-6** is high, biasing transistor Ql on increasing the voltage drop across R26, and biasing transistor Q2 off. When transistor **Q2 is** cut off, **relay 1A1A4K1 is open,** the 28-vdc return circuit **is opened. FAIL power** of 28 vdc is applied from **1A1A4-4 through relay 1A1A4K1-B2** and **B3 to relay 1A1A4K2-X1** causing it to operate and furnish 28 vdc through **1A1A4-7** to light **FAIL lamp 1A1DS1. Latch**out power of 28 vdc enters at 1A1A4-9 **and is** applied through **1A1A4K2-A2 and A1 to latch 1A1A4K2** in the operate condition and maintain the FAIL lamp even if proper operating power returns. It is necessary to set the power mode switch to RESET on STBY to remove the latch-out power furnished by power mode switch 1A1S4B-3 **to 1A1A4-9.** This action allows **1A1A4K2 to restore and 1A1A4K1 to operate before** reapplying latch-out **power to 1A1A4-9.** Resistors R22, R23, and R24 provide failsafe protection against the failure of amplifier-a **Z2 and Z3.**

NOTE

Power control 1A1A4 can light the FAIL lamp in either standby or operate **mode. The operate mode cannot be ac**hieved unless a tdi or cdi unit under test is connected to the indicator test set. The connection of a tdi or cdi unit under test can besimulated by a jumper between **1A1J5-H and J or 1A1J9-s and t. Only** one of these connections need be simulated to operate the indicator test set

2-9. 15-Vdc Power Supply, 1A1A5

The 15-vdc power supply **1A1A5 is identical to** the 15-vdc power supply 7A3 in Detecting Set, Infrared AN/AAS-24. Refer to TM **11-5850-**241-34/1 for a general description of this printed circuit board.

2-10. 15-Vdc Power Supply, 1A1A6

The -15-vdc power supply **1A1A6** is identical to the -15-vdc power supply 7A4 in Detecting Set, Infrared **AN/AAS-24. Refer to TM 11-5850-241-3@** for a general description of this printed circuit board.

2-11. Integrated Circuit Power Supply, 1A1A7

The integrated circuit power supply **1A1A7 identical to the integrated circuits power supply** 7A5 in Detecting Set, Infrared AN/AAS-24. Refer **to TM 11-5850-241-34/1** for a general description of this printed circuit board.

2-12. 150/250-Vdc Power Supply, 1A1A8 (fig. FO-8)

150/250-vdc power supply **1A1A8 provides 150-vdc** regulated power for miscellaneous circuits **1A1A3 and the unit under test. The operation of 1A1A8 is typical of the operation of the 1A1A5, 1A1A6, 1A1A7** regulator boards in the indicator test set.

a. 232-vac, 400-Hz, 3-phase power is applied to a full-wave bridge rectifier consisting of diodes CR1 through CR6. Capacitors C1 through C6 protect the diodes from transient voltage surges. The unregulated dc voltage is applied to external heatsink 1A1A9 and across predrivers Q8 and Q9. Comparator **Z1 has** one input on pin 2 which is the voltage developed across external resistor **1A1R9.** The input to **Z1-3 is** deter**mined by a voltage divider** network consisting of resistor R24, potentiometer R20 **and** external re**sistor 1A1R10. Integrated** circuit Z1 is protected at inputs 2 and 3 by C11 and 12 which by-pass any overload.

b. The preregulator Q1 and resistor R4 form a parallel path to couple the output of **Z1 to** predriver Q9 through pin 23 to external resistor **1A1R7, back into pin 12 to the base of predriver**

Q8. The emitter of the two predrivers develop the drive current to the external heatsink 1A1A9. The two transistors Q1 and Q3 in 1A1A9 regulate the current of the output and dissipate excess heat.

c. The other circuitry on the 150/250-vdc power supply is not used and may be ignored in circuit analysis, as pins 16 and 18 are shorted externally.

2-13. Heatsink Assembly, 1A1A9 (fig. 2-2)

Heatsink assembly 1A1A9 is not a printed circuit board; it is a chassis mounted assembly.

a. Transistors Q2 and Q6 operate in series parallel to regulate the current of the 15-vdc power supply. An increase in load causes a more positive signal at 1A1A9-11 and an increase in current in Q2. This increase is applied to Q6 and the two working together increase the total current to regulate the output voltage at pins **1,** 2, 3, and 4.

b. The two regulating transistors for the 150/250-vdc power supply, Q1 and Q3, operate in an identical manner as Q2 and Q6. The bases are both controlled from the 150/250-vdc power supply and conduct more or less current to maintain a stable output at pin 12.

c. Transistors Q4 and Q5 operate identical to Q2 and Q6. All circuitry and interactions are the same.

2-14. Filter Assembly, 1A1A10 (fig. 2-3)

Filter assembly 1A1A10 protects the indicator test set internal components from induced or power source generated transients. The 115-vac, 400-Hz, 3-phase input power at 1A1J2 is applied across 1A1A10-Rl, R2, R3, and R4 and through FL1 through FL4. The filtered output of FL1 through FL4 is applied through 1A1A10-L2 and L3 and to the three sections of C2. The ac output of **1A1A10** at C2-1 is phase A; C2-2 is phase B; C2-3 is phase C; and C2-4 is neutral. The 28-vdc input at 1A1J1-A is applied through FL5 and L1 to C1. This is the +28-vdc output at E2. The **28-vdc return is 1A1J1-B through FL6 and L1** to C1. The return reference is E3.

2-15. Integrated Circuits

a. Integrated Digital Logic. The 54 series in**tegrated circuits are** high speed, low power, **genera1 purpose circuits for digital applications.** This series includes the basic gates, flip-flop elements and complex logic and storage elements needed to perform all functions of general purpose logic systems. The digital logic circuits employed in the indicator test set are SN5400J, SN5420J, SN5430J, SN5473, and SN5490J. All units in the indicator test set are suffixed by J to denote case style. The SN5400 (A, fig. 2-4) is a quadruple, 2-input positive NAND gate. Four NAND gates with two inputs each, and one output each are *combined in one package. The SN5420 (B, fig. 2-4) is a dual, 4-input positive NAND gate. Two NAND gates with four inputs each, and one output each are combined in one package. The SN5430 is an 8-input positive NAND gate. One NAND gate with eight inputs and one output is in this case. The SN5473 (C, fig. 2-4) is a dual J-K master-slave flip-flop. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the stage of coupling transistors which connect the master and slave sections. The SN5490 (D, fig. 2-4) is a high speed decade counter consisting of four dual-rank, master-slave, flip-flops. When used as a binary coded decimal decade counter, the BD input is externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained. When a symmetric-al divide-by-ten count is desired, requiring division by ten, the D output is externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.

b. Operational **Amplifiers. The operational** amplifiers used in the indicator test set are differential amplifiers and function as summing amplifiers, buffer amplifiers, **and** comparators. **Ter**minal numbers of one amplifier **may be different** from another amplifier as can be seen by comparing the SN52702L and the SN52709L (fig. 2-5 and 2-6) found in the indicator test set. The inverting input is designated (-) while the non-inverting input is **designated (+). Signals applied to the inverting input cause an output signal of opposite polarity to the input. Signals applied to the non-inverting input are reproduced with no inversion. These units are high-performance, general-purpose amplifiers with high-impedance differential inputs and low-impedance outputs.**

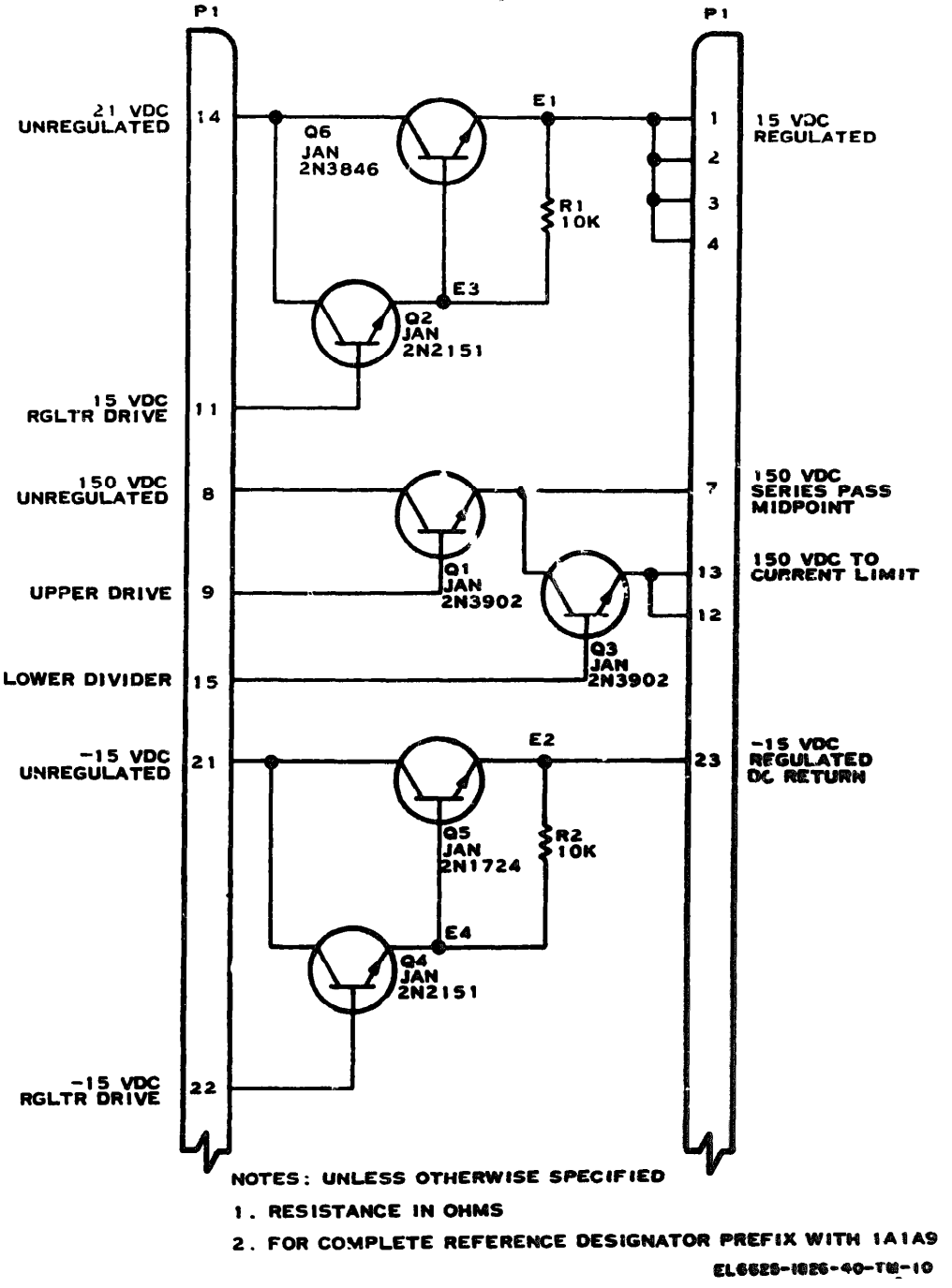


Figure 2-2. Heatsink 1A1A0, schematic diagram.

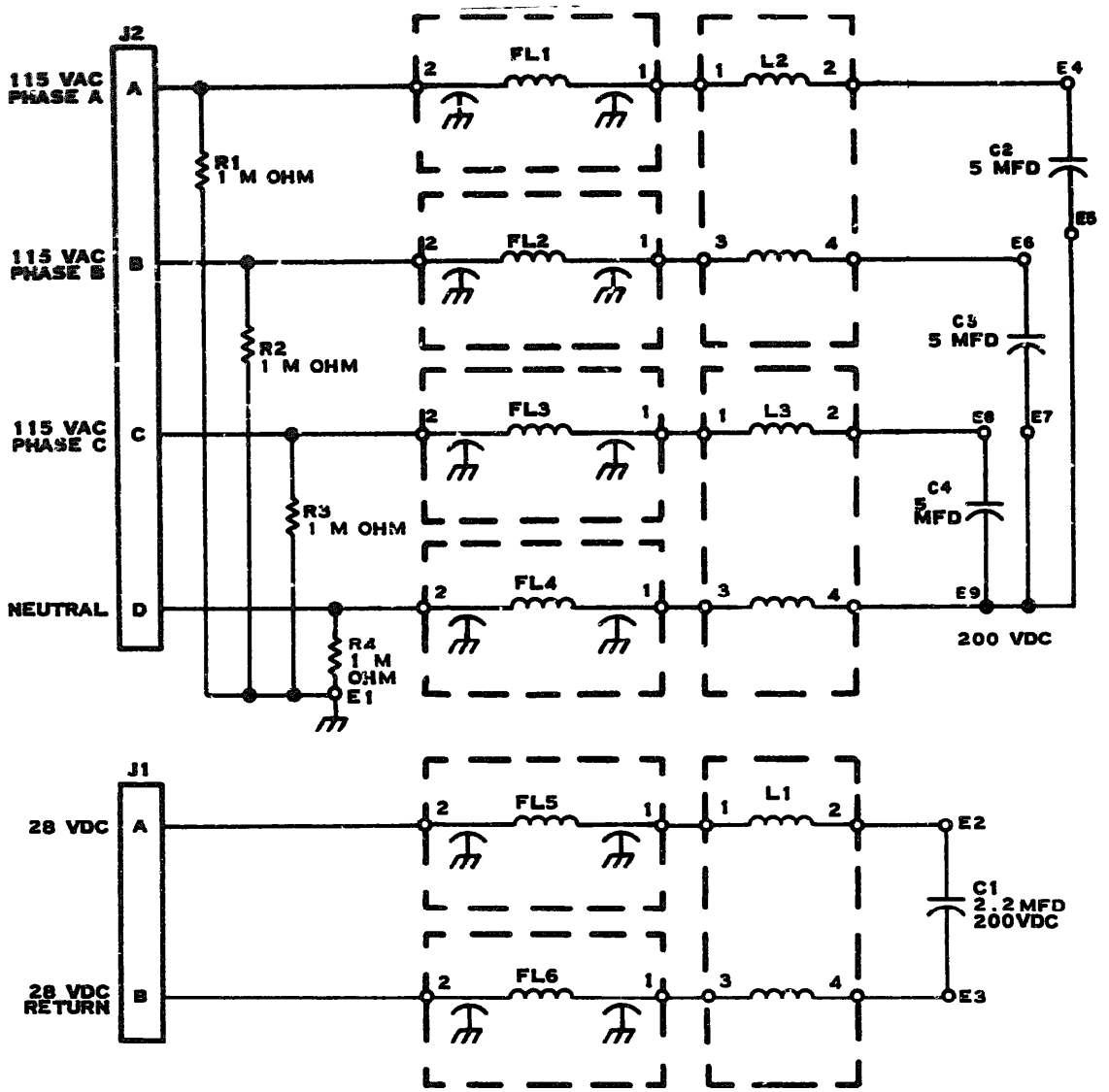


Figure 2-3. Filter Assembly 1a1a10, schematic diagram.

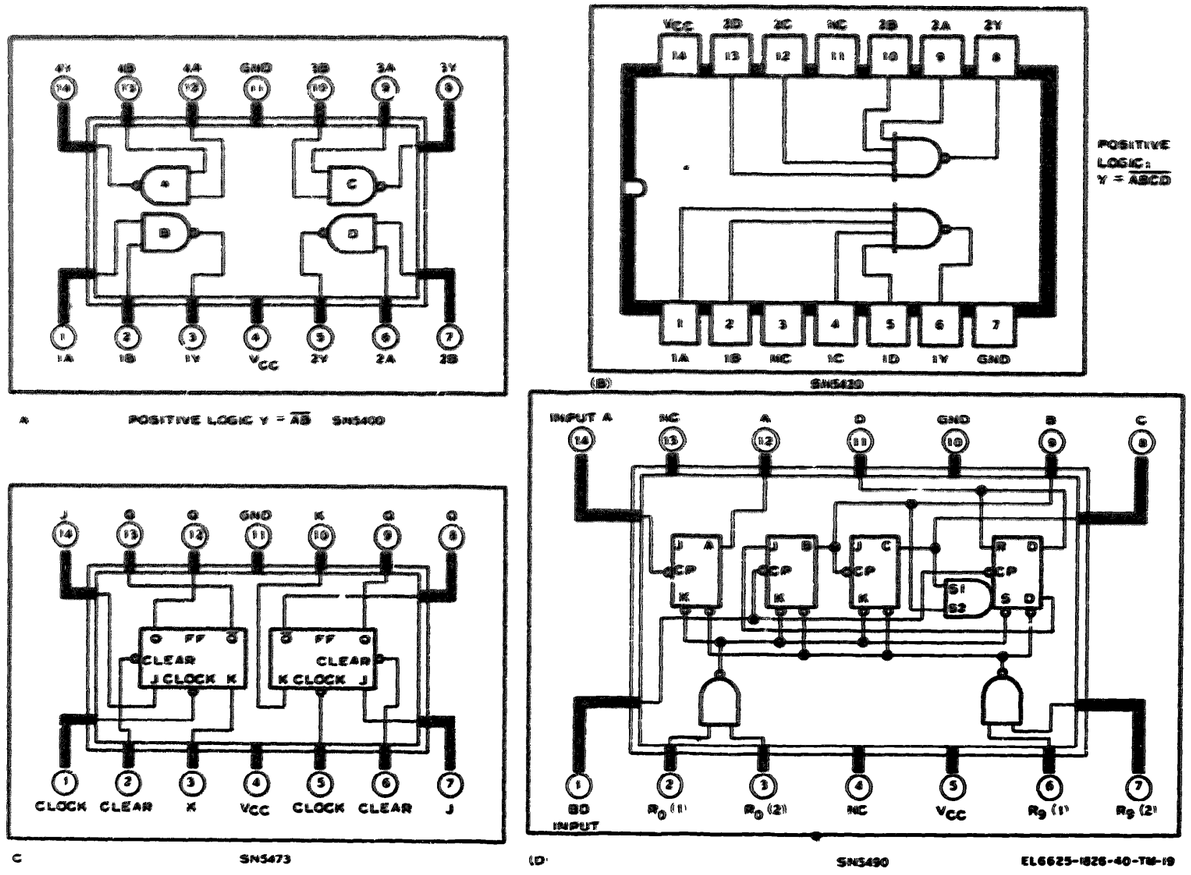


Figure 2-4. Integrated Circuits, types SN5400J, SN5420J, SN5472J, and SN5490J.

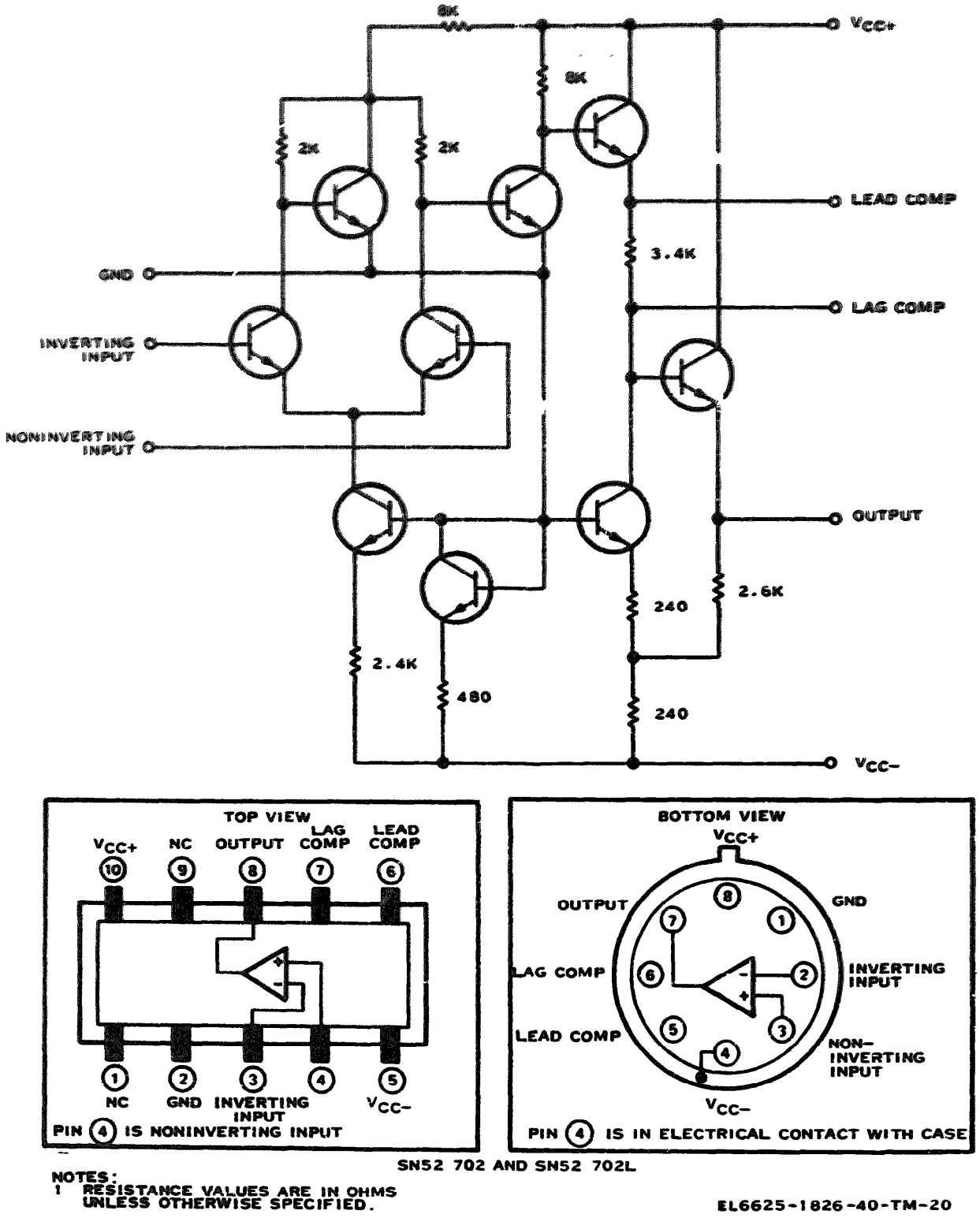


Figure 2-5. Integrated circuit SN52702L.

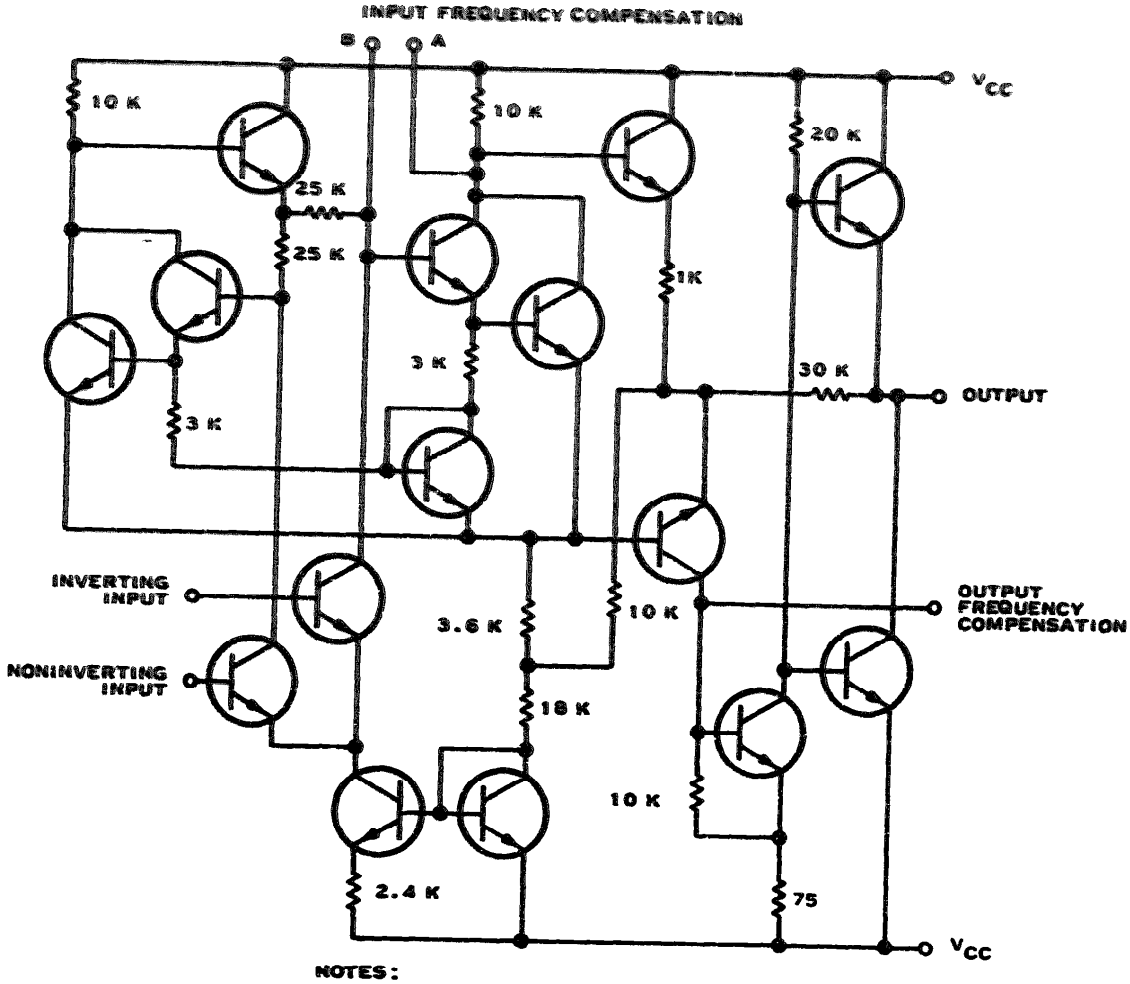


Figure 2-6. Integrated circuit SN52709L.

CHAPTER 3

GENERAL SUPPORT MAINTENANCE

Section I. GENERAL

3-1. Level of Maintenance

This chapter provides general support maintenance procedures. Included in this chapter are sections covering: troubleshooting; removal and replacement; adjustment and alignment; repair; and general support testing.

3-2. Maintenance Forms and Records

Maintenance forms, records, and reports which are to be used by maintenance personnel at all maintenance levels are listed in and prescribed by TM 38–750.

3-3. tools and test Equipment

Tools and test equipment required for maintenance, other than those listed in TM 11–6625–1826–12, are as follows:

a. Tools. Tool Kit, Electronic Equipment TK–105/G.

b. Test Equipment. Test equipment is listed in table 3–1.

Table 3-1. Test Equipmen

Nomenclature	Common name
Oscilloscope AN/USM–281A	Oscilloscope
Digital Voltmeter, Non-Linear Systems, Model X–2	Digital voltmeter (dvm)
Multimeter TS–352B/U	Multimeter
Tool Kit, Electronic Equipment TK–105/G	Tool kit
Maintenance Kit, Electronic Equipment MK–1172/AAS–24	Electronic maintenance kit

c. Digital Voltmeter Preparation for Use. To prepare the digital voltmeter (dvm) for use, connect the power plug to a 115-vac power source (fig. 3–1). Connect the red lead to the HI connector on the dvm panel and the black lead to the LO connector on the dvm panel. Set the power switch to ON. Set the range scale to AUTO.

d. Oscilloscope Preparation for Use. To prepare the oscilloscope for use, connect the power lead to 115-vac power source (fig. 3–1). Connect the oscilloscope test probe to INPUT CH 1 and make a connection between ground on the oscilloscope and GND on the indicator test set. Set the POWER ON switch to the ON position. Position remaining controls as indicated in chart 3–1.

Chart 3-1. Oscilloscope AN/USM-281A Control Settings

Controls	Setting
FIND BEAM	Released.
INTENSITY	As required.
ASTIGMATISM	Use in conjunction with FOCUS to adjust for round beam.
FOCUS	Adjusts beam for sharpest trace.
TRACE ALIGN	Adjusts vertical centering.
SCALE	Adjust for scale illumination.
POWER (indicator)	Signifies POWER switch closed and the 23-vdc power supply is operating.
POWER (switch)	ON (applies ac power to oscilloscope).
HORIZONTAL POSITION	Adjusts horizontal position of display.
DISPLAY	INT.
AC DC	DC.
A POSITION	As required.
POLARITY	+ UP.
DISPLAY	A.
VOLTS/DIV	1.
MAGNIFIER	X1.
CH 1 AC GND DC INPUT	DC.
MAIN VERNIER	CAL.
RESET	Released.
TRIGGER LEVEL	0.
EXT + 10, EXT, INT, LINE	INT.
- SLOPE +	+.
ACS, ACF, AC, DC	DC.
TIME/CM	1 μsec.
SWEEP MODE	AUTO.
DELAY	0.
VERNIER	CAL.
TRIGGER LEVEL	0.
INT, AUTO, EXT, EXT + 10	AUTO.
- SLOPE +	+.
ACS, ACF, AC, DC	DC.

Section II. TROUBLESHOOTING

3-4. General Troubleshooting Instructions

Troubleshooting at the general support maintenance level includes all the techniques outlined for organizational maintenance, and any special or additional techniques required to isolate a defective part. The maintenance procedures are not complete in themselves, but supplement those described in TM 11–6625–1826–12. The systematic troubleshooting procedure, which begins with the operational and sectionalization checks that are performed at an organizational level, must be completed by means of localizing and isolating techniques. The paragraphs that follow provide procedures for sectionalizing troubles to a particular functional unit of the test set, and then to localize the trouble to a component of the functional unit unless the functional unit is replaced and later repaired at a higher level maintenance facility. Waveforms are provided in figure 3–2. Parts location information is provided in figure 3–3. Wiring diagram information and cable diagrams are provided in figures FO–9 and FO–10. Color codes for resistors, inductors, and capacitors are provided in figure FO–1. The wire color code shown on wiring diagrams is the same numerical code explained in *figure FO-1.*

3-5. Organization of Troubleshooting

a. General. The first step in troubleshooting is to sectionalize the fault (tracing the fault to a major functional unit). The second step is to localize the fault (tracing the fault to a defective part within that unit). Some faults, such as burned-out resistors, arcing, and shorted transformers can often be located by sight, smell, and hearing. The majority of faults however, must be isolated by checking voltages and resistances, or by checking the equipment against the general support test procedure contained in section VI of this chapter.

b. Sectionalization. For ease of troubleshooting, the equipment may be thought of as consisting of functional entities, each related eletrically but categorized separately by the function performed. The first step in troubleshooting is to *locate* the function, or functions, at fault by the following methods:

(1) Visual inspection. The purpose of the visual inspection is to locate faults without testing or measuring the circuits. All visual signs should be observed and an attempt made to sectionalize the fault to a particular function.

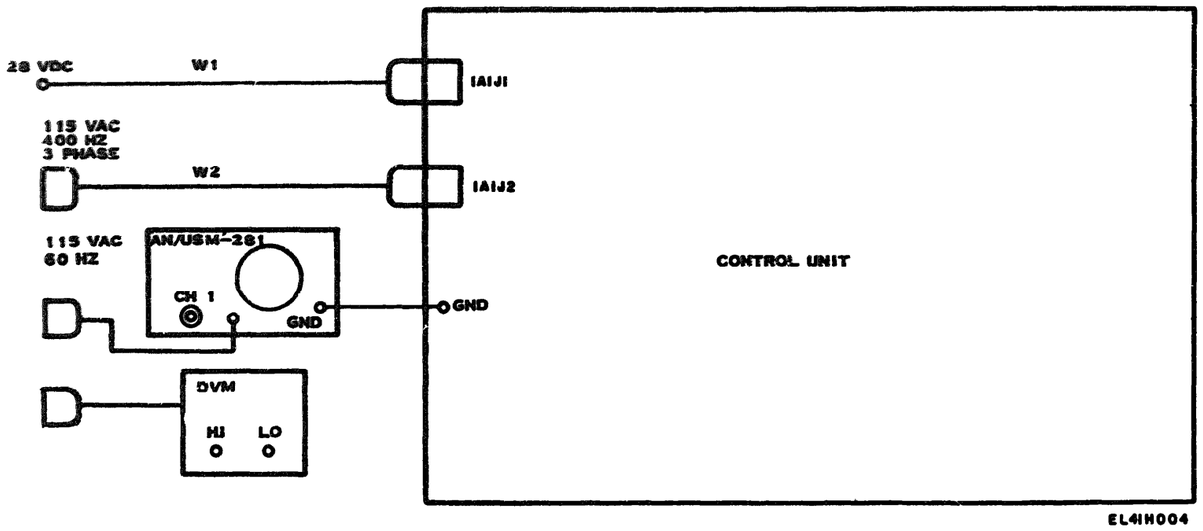


Figure 3-1. test setup.

(2) *Operational test.* Operational test frequently indicate the general location of trouble. In many instances the tests will help in determining the exact nature of the fault. The organizational quarterly preventive maintenance checks and service chart (TM 11-6625-1826-12) contains an operational test.

c. Localization. The tests listed in the following paragraphs will aid in localizing the trouble. First, localize the trouble to a single function, and then isolate the trouble within that circuit by waveform, voltage, resistance, and continuity measurements.

(1) *Troubleshooting chart.* When used with the associated voltage, resistance, and continuity tables and the waveform diagram, the troubleshooting information in chart 3-2 will aid the technician in localizing troubles to a component part. Defective components identified by performing the corrective action are replaced with a known reliable component unless repair or other disposition is noted. The *Corrective action* column references data tables, if required, for checking components; otherwise refer to schematic and wiring diagrams when performing checks. The parenthetical reference in the *Malfunction* column is intended to be used only when performing the general support test procedure. The referenced data items and test procedure steps will allow malfunction symptoms discovered during performance of the test procedure to be easily referenced in the troubleshooting chart.

(2) *Waveform measurements (fig. 3-2).* Oscilloscope, AN/USM-281A is used for observing waveforms at appropriate test points. The waveform chart on figure 3-2 illustrates the waveforms obtained at various points on the chassis.

Chart 3-2. Troubleshooting Procedure

Note: Adjust and align appropriate PCB before replacing.

m No.	Malfunction	Probable cause	Corrective action
1	FAIL lamp 1A1DS1 lights	a. Power fluctuation	a. Set power mode switch to reset and release.
		b. Loss of 115-vac input power	b. Check CB2. Reset if tripped.
		c. Loss of one or more phases of 115 vac input power.	c. Check input power.
		d. No input to power transformer 1A1T1.	d. Check power relay 1A1K1 (para 3-5c(3); table 3-3, item 1).
		e. Incorrect output of power transformer 1A1T1.	e. Check power transformer 1A1T1 (para 3-5c(3); table 3-2, items 10 through 21).
		f. Faulty input to power control 1A1A4.	f. Perform the following:
		(1) No +15 vdc at 1A1A4-16	(1) Check 1A1A5, pin 2, for +16.4 ±0.4 vdc. If present, check 1A1J11, pin 2, for +15 ±0.3 vdc.
		(2) No +5 vdc at 1A1A4-14	(2) Check 1A1A7, pin 3, for +5 ±0.1 vdc. If present, check 1A1K4, pin A1, for +5 ±0.1 vdc.
		(3) No +150 vdc at 1A1A4-18	(3) Check 1A1A8, pin 10, for +325 ±30 vdc. If present, check 1A1A9, pin 12, for +150 ±3 vdc.
		(4) No −15 vdc at 1A1A4-20	(4) Check 1A1A6, pins 13 and 6 for −15 ±0.3 vdc. If present, check 1A1J11, pin 22, for +1.4 ±0.4 vdc.
		(5) No +15 vdc at 1A1A4-1	(5) Check continuity between 1A1J11-2 and 1A1A4-1.
		(6) No −15 vdc at 1A1A4-22	(6) Check continuity between 1A1A4-1 and 1A1A6-2.
		g. Faulty heatsink, 1A1A9	g. Check heatsink 1A1A9 (malfunctions 9, 10, and 11).
		h. Faulty power control 1A1A4	h. Replace 1A1A4.

Item No.	Malfunction	Probable cause	Corrective action
2	ELAPSED TIME meter 1A1M1 does not operate.	a. 1A1CB2 faulty b. Faulty relay 1A1K1 c. ELAPSED TIME meter 1A1M1 defective.	a. Check 1A1CB2. b. Check 1A1K1 (para 3-5c(3); table 3-3, item 1). c. Check 1A1M1 for resistance of 2 ±0.5 ohms.
3	STBY lamp 1A1DS2 does not light.	a. Defective circuit breaker 1A1CB1 b. Diode 1A1CR1 open c. Relay 1A1K1 defective d. Power mode switch 1A1S4 defective. e. STBY lamp 1A1DS2 defective	a. Check 1A1CB1. b. Check 1A1CR1 (para 3-5c(3); table 3-2, items 26 and 27). c. Check 1A1K1 (para 3-5c(3), table 3-3, item 1). d. Check 27 ±2 vdc at 1A1K1-X1. e. Check 1A1DS2.
4	OPR lamp does not light	a. Relay 1A1K2 defective b. OPR lamp 1A1DS3 defective. Relay 1A1K2 defective.	a. Check 1A1K2 (para 3-5c(3); table 3-3, item 2). b. Check 1A1DS3.
5	No 115 vac, 3 phase, 400 Hz at J5 and J9-A, B, and C. FAIL lamp is not lighted.	Relay 1A1K3 defective	Check 1A1K2 (para 3-5c(3); table 3-3, item 2).
6	No +5 vdc present at J5-CC in operate mode.	Relay 1A1K3 defective	Check 1A1K3 (para 3-5c(3); table 3-3, item 2).
7	No −15 vdc present at J5-Z, c, f, DD, J4-J or J3-C.	Relay 1A1K3 defective	Check 1A1K3 (para 3-5c(3); table 3-3, item 3)
8	No +15 vdc present at J5-a, d, g, EE, J4-H or J3-A.	Relay 1A1K3 defective	Check 1A1K3 (para 3-5c(3); table 3-3, item 2).
9	+15 vdc at output of heatsink 1A1A9-1, 2, 3, 4 not present or not in tolerance (table 3-2, item 2).	a. +15 vdc power supply 1A1A5 defective. b. Heatsink 1A1A9 defective	a. Check 1A1A5, pin 2, for +15 ±0.3 vdc. b. Replace 1A1A9.
10	−15 vdc at output of heatsink 1A1A9-23 not present or not in tolerance (table 3-2, item 4).	a. −15 vdc power supply 1A1A6 defective. b. Heatsink 1A1A9 defective	a. Check 1A1A6, pins 13 and 6 for −15 ±0.3 vdc. b. Replace 1A1A9.
11	+150 vdc at output of 1A1A9-12 not present or not in tolerance (table 3-2, item 1).	a. +150 vdc power supply 1A1A8 defective. b. Heatsink 1A1A9 defective	a. Check 1A1A8, pin 10, for +325 ±30 vdc. b. Replace 1A1A9.
12	+5 vdc at TB1-6 not present or not in tolerance (table 3-2, item 5).	+5 vdc power supply 1A1A7 defective	Check 1A1A7, pins 1 and 3 for +5 ±0.1 vdc.
13	Indicator test set does not go into operate mode and FAIL lamp does not light.	Jumper between TEST POINTS 6 and TEST POINTS 7 defective.	Check jumper.
14	No continuity from TEST POINTS 1 to J7-F, J, K, L, J6-H, C or J5-K (table 3-4, items 1 through 7).	TEST POINTS switch 1A1S7 defective.	Check 1A1S7-A (para 3-5c(3); table 3-4, items 1 through 7).
15	No continuity from TEST POINTS 2 to J4-S, J6-E, F or J5-AA (table 3-4, items 8 through 11).	TEST POINTS switch 1A1S7 defective.	Check 1A1S7-B (para 3-5c(3); table 3-4, items 8 through 11).
16	No continuity from TEST POINTS 3 to J9-Z, a, b, c, u, J5-y or J4-R (table 3-4, items 12 through 18).	TEST POINTS switch 1A1S7 defective.	Check 1A1S7-C (para 3-5c(3); table 3-4, items 12 through 18).
17	No continuity from TEST POINTS 4 to J4-d, G, J5-s, z, J9-V, Y (table 3-4, item 19).	TEST POINTS switch 1A1S7 defective.	Check 1A1S7-D (para 3-5c(3); table 3-4, items 19 through 24).

Item No.	Malfunction	Probable cause	Corrective action
18	No continuity from TEST POINTS SCOPE to J3-D or J6-K.	TEST POINTS switch 1A1S7 defective.	Check 1A1S7-E (para 3-5c(3); table 3-4 items 25 and 26).
19	No +150 vdc at TEST POINTS 1 with TEST POINTS switch 1A1S7 set to 1 (table 3-2, item 1).	TEST POINTS switch 1A1S7 defective.	Check 1A1S7-A contact 1 for 150 ±15.0 vdc.
20	No +15 vdc at TEST POINTS 2 with TEST POINTS switch 1A1S7 set to 1 (table 3-2, item 2).	TEST POINTS switch 1A1S7 defective.	Check 1A1S7-B contact 1 for 15.0 ±1.5; −0.0 vdc.
21	No −15 vdc at TEST POINTS 3 with TEST POINTS switch 1A1S7 set to 1 (table 3-2, item 4).	TEST POINTS switch 1A1S7 defective.	Check 1A1S7-C contact 1 for 15.0 +0.0; −1.5 vdc.
22	No +5 vdc at TEST POINTS 4 with TEST POINTS switch 1A1S7 set to 1 (table 3-2, item 5).	TEST POINTS switch 1A1S7 defective.	Check 1A1S7-D contact 1 for 5.0 ±0.5 vdc.
23	Video intensity incorrect at SCOPE with TEST POINTS switch in 1 (table 3-2, item 6).	Video processor 1A1A2 defective	Check 1A1A2, pin 23, para 3-5c(3); table 3-2, item 6.
24	Reticle ramp waveshape incorrect at TEST POINTS SCOPE with TEST POINTS switch 1A1S7 in position 2 (chart 3-3, step No. 11).	a. Video generator 1A1A1 defective	a. Check 1A1A1, pin 2, for waveform H, figure 3-2.
		b. Miscellaneous circuits 1A1A3 defective.	b. Check 1A1A3, pin 19, for waveform A, figure 3-2. FIELD OF VIEW: X1, VIDEO SELECT: OFF.
25	Tdi step waveshape incorrect (chart 3-3, step No. 12).	a. FIELD OF VIEW switch 1A1S3 defective.	a. Check 1A1S3AC1-1 for +5.6 ±1.0 vdc. PATTERN switch: 3.
		b. PATTERN switch 1A1S1 defective	b. Check 1A1S1 for continuity between 1A1S1B-3 and 1A1S1B-C1.
		c. Video generator 1A1A1 defective	c. Check 1A1A1, pin 23, waveform G, figure 3-2.
		d. 5 volt waveform out of tolerance.	d. See Section IV, p. 3-16, for adjustment procedure.
		e. Miscellaneous circuits 1A1A3 defective.	e. Check 1A1A3, pin 2, for waveform B, figure 3-2.
26	Read vertical sync waveform incorrect (chart 3-3, step No. 13).	a. FIELD OF VIEW 1A1S3 position 1 defective.	a. Check 1A1S3.
		b. PATTERN switch 1A1S1 defective position 3.	b. Check 1A1S1.
		c. Video generator 1A1A1 defective	c. Check 1A1A1, pin 23, for waveform G, figure 3-2.
27	Video gate waveform incorrect (chart 3-3, step No 14).	a. INPUT switch 1A1S5 defective	a. Check 1A1S5-B7 and 3 for +15 ±0.3 vdc.
		b. Video generator 1A1A1 defective	b. Check 1A1A1, pin 6, for waveform I, figure 3-2.
28	Tdi horizontal sync waveform incorrect at J7-i (chart 3-3, step No. 15).	a. Video generator 1A1A1 defective	a. Check 1A1A1, pin 2, for waveform H, figure 3-2.
		b. Miscellaneous circuits 1A1A3 defective.	b. Check 1A1A3-16 and -17 for waveform E, figure 3-2.
29	Tdi video waveform at TEST POINTS INP VID incorrect (chart 3-3, step No. 16).	a. Defective VIDEO SELECT switch 1A1S6.	a. Check 1A1S6 for +3.3 ±0.6 vdc.
		b. Defective PATTERN switch 1A1S1.	b. Check 1A1S1 for continuity between A1S1A-C1 and 1A1S1A-4.
		c. Defective video generator 1A1A1	c. Check 1A1A1, pin 17, for waveform J, figure 3-2.
		d. Incorrect video intensity 1A1R1 level.	d. Check 1A1R1 (para 3-5c(3); table 3-2, item 6).
		e. Video processor 1A1A2 defective.	e. Replace 1A1A2.
30	Video 1, 2, 3, or 4 at J8-U, R, or N and J6-e missing video.	a. CAL IND CONTROLS INPUT switch 1A1S5 defective.	a. Check 1A1S5-A.

Item No.	Malfunction	Probable cause	Corrective action
	present at TEST POINTS INP VIDEO (chart 3-3, steps No. 16, 17, 18 and 19)	b. Video processor 1A1A2 defective	b. Observe waveform F, figure 3-2, at 1A1XA2-12, 6, 2, and 10; TEST POINTS switch in positions 1, 2, 3, and 4.
31	Video 1, 2, 3, or 4 at J6-e or J8-U, R, or N incorrect waveform (chart 3-3, steps No. 16, 17, 18, and 19).	Refer to probable cause of malfunction 29.	Refer to corrective action of malfunction 29.
32	Vertical sync 1A1A1-19, not present or incorrect, TEST POINTS 20 (chart 3-3, step No. 20).	Defective video generator 1A1A1	Replace 1A1A1.
33	Filter assembly 1A1A10 does not have continuity from 1A1J1-A and B to 1A1A10-E2 and E3 and from 1A1J2-A, B, C and D to 1A1A10C2-1, 2, 3 and 4.	a. Defective choke coil 1A1A10-L1, L2 or L3. b. Defective filter 1A1A10-FL-1, 2, 3, 4, 5 or 6. c. Broken wiring	a. Check coils 1A1A10-L1, L2, or L3 for continuity. b. Check filters 1A1A10-FL-1, 2, 3, 4, 5, and 6 for continuity. c. Check wiring.
34	Continuity is present between connector pins 1A1J2-A, B, C, D or 1A1J1-A to 1A1E1.	Shorted or defective wiring	Check wiring.

(3) *Voltage and resistance measurements.* The digital voltmeter, Nonlinear System, Model X-2, is used for taking voltage and resistance measurements on the chassis. Multimeter TS-352B/U is available if required. Voltage measurements are listed in table 3-2 and resistance measurements are listed in table 3-3. The item column is provided so specific measurements can be easily referenced. The *Component checked* column designates which component can be checked by using the data provided for that item. The dvm probe connections LO and HI columns specify where the HI probe and LO probe are connected to check the corresponding item component. The test set control setting control and position columns designate test unit control settings which must be made prior to observing the dvm indication for the item checked. The dvm indication (volts) dc and ac column on the voltage measurement table (table 3-2) contains the dvm dc or ac voltage obtained for the item component checked. The dvm indication (ohms) on the resistance measurement table (table 3-3) contains the resistance obtained for the item checked. Unless otherwise specified, tolerances are ±10 percent. Chassis mounted components requiring resistance checks must be isolated from associated circuits to avoid erroneous meter indications.

CAUTION

When making voltage measurements of transistors, use tape or sleeving to insulate the test probe, except for the extreme tip, to prevent accidental shorting of the test probes to the chassis (even a momentary short circuit can damage the transistor).

Table 3-2. Voltage Measurements

Item	Component checked	Dvm probe connection		Test set control setting		Dvm indication (volts)	
		LO	HI	Control	Position	Ac	Dc
1	1A1A8	Test point 8	Test point 1	TEST POINTS Switch S7	1		150±3
2	1A1A5	Test point 8	Test point 2	S7	1		15±0.3
3	1A1R3	Test point 8	Test point 2	S7	3		
				BRIGHTNESS control			
				1A1R3	Fully cw		80±8
				1A1R2	Fully ccw		10±2

Item	Component checked	Dvm probe connection		Test set control setting		Dvm indication (volts)	
		LO	HI	Control	Position	A±	B±
		Test point 8	J-4Z	S7	8		
				1A1R3	Fully ccw		10±2
				1A1R3	Fully cw		80±8
4	1A1A6	Test point 8	Test point 3	S7	1		−15±0.3
5	1A1A7	Test point 8	Test point 4	S7	1		+5 ±0.1
6	1A1R1	Test point 8	Test point SCOPE	S7	1		
				VIDEO INTENSITY			
				1A1R1	Fully cw		−8±0.5
				1A1R1	Fully ccw		−6±0.5
7	1A1T1	T1-N	T1-1			119±12	
8	1A1T1	T1-N	T1-2			119±12	
9	1A1T1	T1-N	T1-3			119±2	
10	1A1T1	1A1T1-5	1A1T1-4			28.8±4	
11	1A1T1	1A1T1-5	1A1T1-6			28.8±4	
12	1A1T1	1A1T1-4	1A1T1-6			28.8±4	
13	1A1T1	1A1T1-7	1A1T1-8			21.6±4	
14	1A1T1	1A1T1-7	1A1T1-9			21.6±4	
15	1A1T1	1A1T1-8	1A1T1-9			21.6±4	
16	1A1T1	1A1T1-13	1A1T1-14			11.2±3	
17	1A1T1	1A1T1-13	1A1T1-15			11.2±3	
18	1A1T1	1A1T1-14	1A1T1-15			11.2±3	
19	1A1T1	1A1T1-10	1A1T1-11			240±24	
20	1A1T1	1A1T1-10	1A1T1-12			240±24	
21	1A1T1	1A1T1-11	1A1T1-12			240±24	
22	Filter 1A1A10	1A10-E9	1A10-E4			119±12	
23	Filter 1A1A10	1A10-E9	1A10-E6			119±12	
24	Filter 1A1A10	1A10-E9	1A10-E8			119±12	
25	Filter 1A1A10	1A10-E3	1A10-E2				27±2
26	1A1CR1	TB1-1	E4				27.5±3
27	1A1CR1	TB1-1	E5				26.7±3
28	1A1S3-B	Test Point 8	J4-V	Switch 1A1S3	X1 or X2		−15 ± 0.3
29	1A1S3-B	Test Point 8	J4-W	Switch 1A1S3	X1		−15 ± 0.3

Table 3-3. Resistance Measurements

Item	Component checked	Dvm probe connection		Test set control setting		Dvm indication (ohms)
		LO	HI	Control	Position	
1	1A1K1	1A1K1-X2	1A1K1-X1			290±30
2	1A1K2	1A1K2-X2	1A1K2-X1			290±30
3	1A1K3	1A1K3-X2	1A1K3-X1			290±30
4	1A1K4	K4-N	K4-φC			100k min
		K4-N	K4-φB			100k min
		K4-N	K4-φA			100k min
5	1A1R1	1A1R1-1	1A1R1-3		Remove 1A1A2	1000±150
		1A1XA2-14	1A1XA1-23	1A1R1	cw	Less than 5
		1A1XA2-14	1A1XA1-23	1A1R1	ccw	1000±150
6	1A1R2	1A1R2-1	1A1R2-3		(Install 1A1A2)	1000±150
		J7-S	J7-T	1A1R2	Fully ccw	1000±150
		J7-S	J7-T	1A1R2	Fully cw	Less than 5
7	1A1R3	1A1R3-1	1A1R3-3			100±10k
		1A1R3-1	J4-Z	1A1R3	Fully ccw	100±10k

Item	Component checked	Dvm probe connections		Test set control setting		Dvm indication (ohms)
		LO	HI	Control	Position	
		1A1E2-1	J4-Z	1A1E2	Fully cw	Less than 5
8	1A1E4	1A1E4-1	1A1E4-3			1025 ± 103
		J4-a	J4-c	1A1E4	Fully ccw	Less than 11
		J4-3	J4-c	1A1E4	Fully cw	1033 ± 103
9	1A1E5	1A1E5-1	1A1E5-2			75±1
10	1A1E6	1A1E6-2	1A1E6-1			12k ±0.12k
11	1A1E7	1A1E7-2	1A1E7-1			12k ±0.12k
12	1A1E8	1A1E8-1	1A1E8-2	COMMENT:	Remove 1A1A8	8k ±0.08k
13	1A1E9	1A1E9-1	1A1E9-2			12.7k ±0.13k
14	1A1E10	1A1E10-E2	1A1E10-E3			80.6k ±0.80k
15	1A1E11	1A1E11-1	1A1E11-2			51.1 ± 1
16	1A1CR1	Cathode	Anode	COMMENT:	Replace 1A1A8	Less than 50
	through	Anode	Cathode			Greater than 250k
	1A1CR8					
17	A10-E5	A10-E4				350K
18	A10-E5	A10-E6				350K
19	A10-E5	A10-E8				350K

(4) *Continuity checks.* Routine continuity checks between various points in the circuitry can be made using the digital voltmeter or the multimeter and wiring diagrams; however, a list of continuity checks is provided in table 3-4 to insure a complete continuity check of the circuitry without reference to wiring diagram. The continuity measurements table *Item* column is provided so specific measurements can be easily referenced. The *Dvm probe connections LO* and *HI* columns specify where the dvm HI probe and LO probe are connected to check the corresponding item continuity measurements. The *Test unit control setting, Control* and *Position* columns designate test unit control settings which must be made prior to observing the dvm indication for the item circuitry checked. The *Remarks* column contains information of a special nature pertinent to checking continuity for the specific corresponding item. Continuity is defined as a continuous path with a resistance of less than 2 onms unless otherwise noted. All measurements are made with power off and circuit breakers open. Prefix all designators with 1A1.

Table 3-4. Continuity Measurements

Item	Dvm probe connection		Test unit control settings		Remarks
	LO	HI	Control	Position	
1	Test point 1	J7-H	TEST POINTS Switch S7	2	
2	Test point 1	J7-J	S7	3	
3	Test point 1	J7-K	S7	4	
4	Test point 1	J7-L	S7	5	
5	Test point 1	J6-H	S7	6	
6	Test point 1	J5-K	S7	7	
7	Test point 1	J6-C	S7	8	
8	Test point 2	J6-E	S7	5	
9	Test point 2	J6-F	S7	6	
10	Test point 2	J5-AA	S7	7	
11	Test point 2	J4-S	S7	8	
12	Test point 3	J9-Z	S7	2	
13	Test point 3	J9-a	S7	3	
14	Test point 3	J9-b	S7	4	
15	Test point 3	J9-c	S7	5	
16	Test point 3	J9-U	S7	6	
17	Test point 3	J5-y	S7	7	
18	Test point 3	J4-R	S7	8	
19	Test point 4	J4-d	S7	3	
20	Test point 4	J5-s	S7	4	

Item	Dmm probe connection		Test unit control settings		Remarks
	LO	HI	Control	Position	
21	Test point 4	J9-V	S7	5	
22	Test point 4	J9-Y	S7	6	
23	Test point 4	J5-a	S7	7	
24	Test point 4	J4-G	S7	8	
25	SCOPE	J8-D	S7	7	
26	SCOPE	J6-K	S7	8	
27	Test point 6	TB1-1			inf
28	J2-A	A10-E4			
29	J2-B	A10-E6			
30	J2-C	A10-E8			
31	J2-D	A10-E5			
32	J1-A	A10-E2			
33	J1-B	A10-E3			
34	J2-A	TB1-1			
35	J2-B	TB1-1			inf
36	J2-C	TB1-1			inf
37	J2-D	TB1-1			inf
38	TB1-1	J9-G	1A1S5	1 or 2	
39	TB1-1	J9-H	1A1S5	1 or 2	
40	TB1-1	J9-F	1A1S5	1	

(5) ***Intermittent troubles.*** **When troubleshooting, the possibility of intermittent troubles should not be overlooked. This trouble can often be made to appear by tapping or jarring the equipment. Check wiring and connections.**

3-6. Interunit Troubleshooting

a. Defective Signal Monitoring. **Failure to monitor a selected voltage or signal may be caused by defective external test equipment. If an operational check fails to sectionalize trouble to a defective unit or a defective major functional area, follow the procedures given in (1), (2), and (3) below.**

(1) ***External test equipment check.*** **All external test equipment should function properly. Perform operational checks on each unit of external test equipment as described in the applicable test equipment manual.**

(2) ***Control units check.*** **All major functional areas of the control units should function properly, including the active circuits (semiconductor circuits) and the controls.**

(a) ***Active circuits.*** **If any of the transistor or diode circuits are suspected of causing a malfunction, isolate the trouble by using voltage and resistance measurements with external test equipment.**

(b) ***Controls.*** **To verify that all controls are functioning properly, perform continuity measurements (table 3–4) while the controls are rotated through each position.**

(3) ***Connectors check.*** **The continuity measurements will aid in determining whether a connector is contributing to the malfunction.**

b. Checking Cable Assemblies. **All interconnecting cable assemblies should be checked for signs of insulation deterioration and for opens or shorts near the connectors. Check connectors for bent or deformed pins and for signs of arcing.**

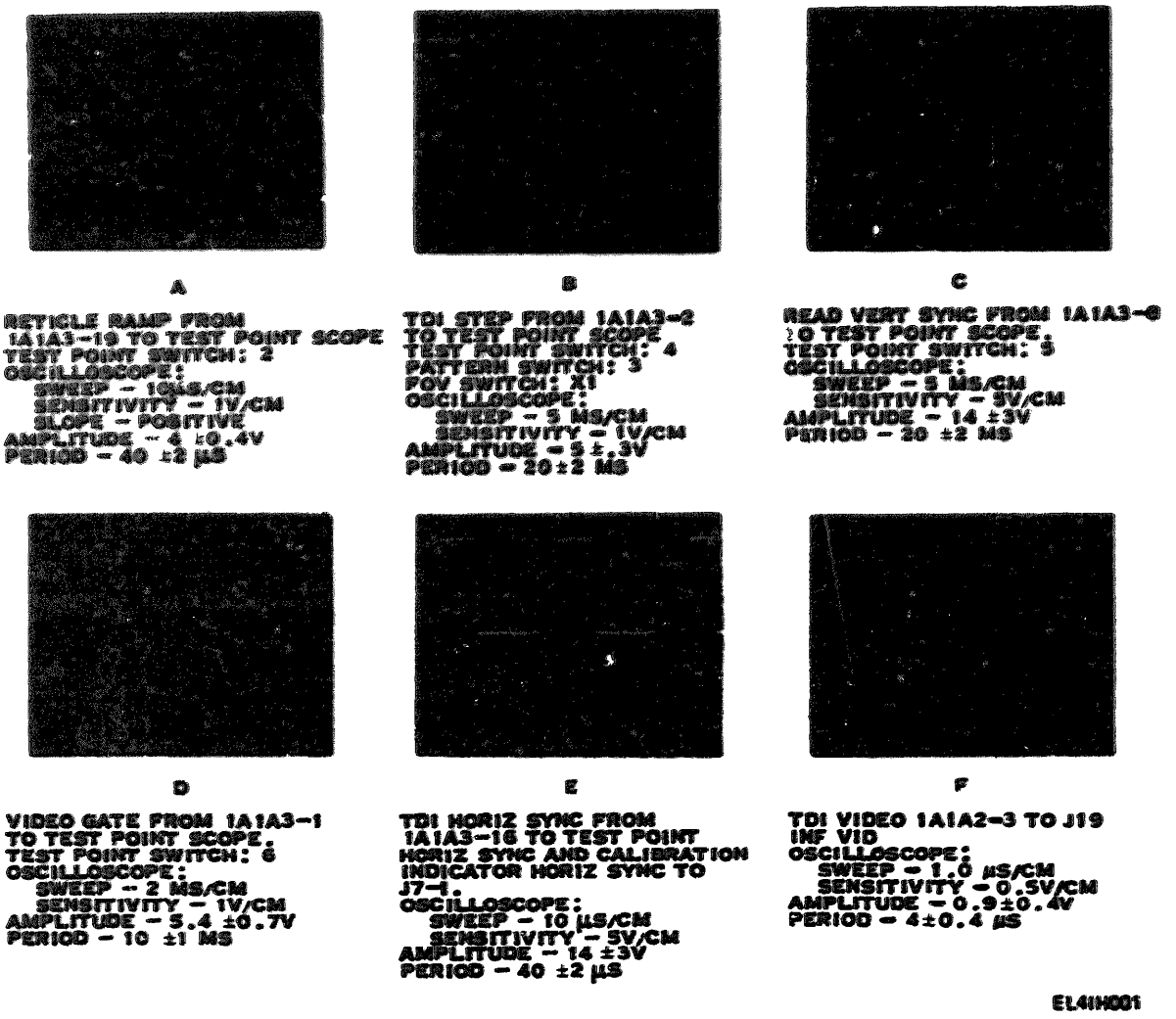
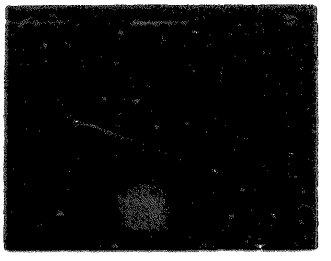


Figure 3-2(1). Waveforms (part 1 of 2).

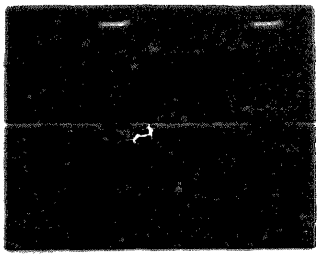
G

VERTICAL SYNC 60 HZ,
1A1A1-19 OR 23.
OSCILLOSCOPE:
SWEEP - 5 MS/CM
SENSITIVITY - 5V/CM
AMPLITUDE - 14 ±3V
PERIOD - 20 ±2 MS



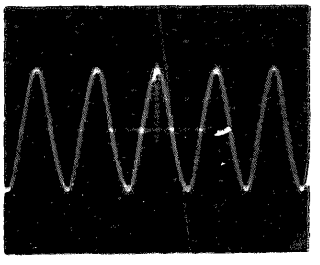
H

25 KHZ OUTPUT 1A1A1-2
OSCILLOSCOPE:
SWEEP - 10 µS/CM
SENSITIVITY - 1V/CM
AMPLITUDE - 3.4 ±1V
PERIOD - 40 ±2 µS



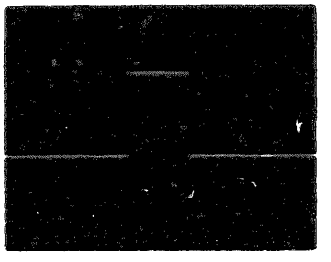
I

100 HZ OUTPUT, 1A1A1-6
OSCILLOSCOPE:
SWEEP - 2 MS/CM
SENSITIVITY - 1V/CM
AMPLITUDE - 3.4 ±1V
PERIOD - 10 ±1 MS



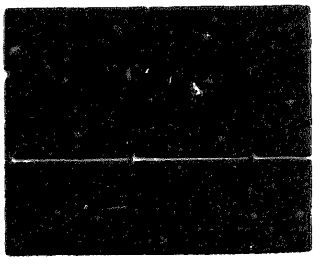
J

VIDEO 1A1A1-17
OSCILLOSCOPE:
SWEEP - 0.05 µS/CM
SENSITIVITY - 1V/CM
AMPLITUDE - 3 ±1V
PERIOD - 0.1±0.01 µS



K

LINEARITY AND RETICLE
COMMAND 1A1A1-17
OSCILLOSCOPE:
SWEEP - 20 µS/CM
SENSITIVITY - 1V/CM
X10 MAGNIFIER
EXTERNAL TRIGGER - VERT
SYNC FROM TEST SET
AMPLITUDE - 3.4 ±1V
PULSE WIDTH - 40 ±4 µS



L

INTERLACE AND RETICLE
COMMAND 1A1A1-17
OSCILLOSCOPE:
SWEEP - 1 µS/CM
SENSITIVITY - 1V/CM
AMPLITUDE - 3.4 ±1V
PERIOD - 4 ±0.4 µS

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Figure 3-2(2). Waveforms (part 2 of 2).

Section III. Removal and Replacement

3-7. Removal

All parts may be removed using standard tools and maintenance procedures. Refer to parts location diagram (fig. 3-3), when removing parts and subassemblies.

a. The control unit is removed by disengaging the screws along the edge of the panel and sliding the chassis from the case.

b. Access to printed circuit boards is gained by removing the 5 captive screws securing the hinged cover and swinging it open.

c. To gain access to the remaining chassis mounted components, remove the 6 captive screws securing the two hinged portions of the chassis and swing open.

d. Access to the filter assembly is gained by removing the two retaining nuts securing 1A1J1 and 1A1J2 to the panel and removing the 8 panhead screws securing the filter assembly case to the control unit panel. Refer to parts location diagram (fig. 3-4), when removing parts and subassemblies.

3-8. Replacement

All parts may be replaced using standard tools and maintenance procedures. Refer to part location diagram (fig. 3-3), when replacing parts and subassemblies.

a. The control unit is replaced by sliding the chassis back into the case and securing the screws along the edge of the panel.

b. Secure the printed circuit board hinged cover with the 5 captive screws.

c. Secure the hinged portions of the chassis with the 6 captive screws.

d. To replace the filter assembly, secure J1 and J2 to the control unit panel with the two retaining nuts; secure the filter assembly case to the control unit panel with the 8 panhead screws. Refer to the part location diagram (fig. 3-4), when replacing parts and subassemblies.

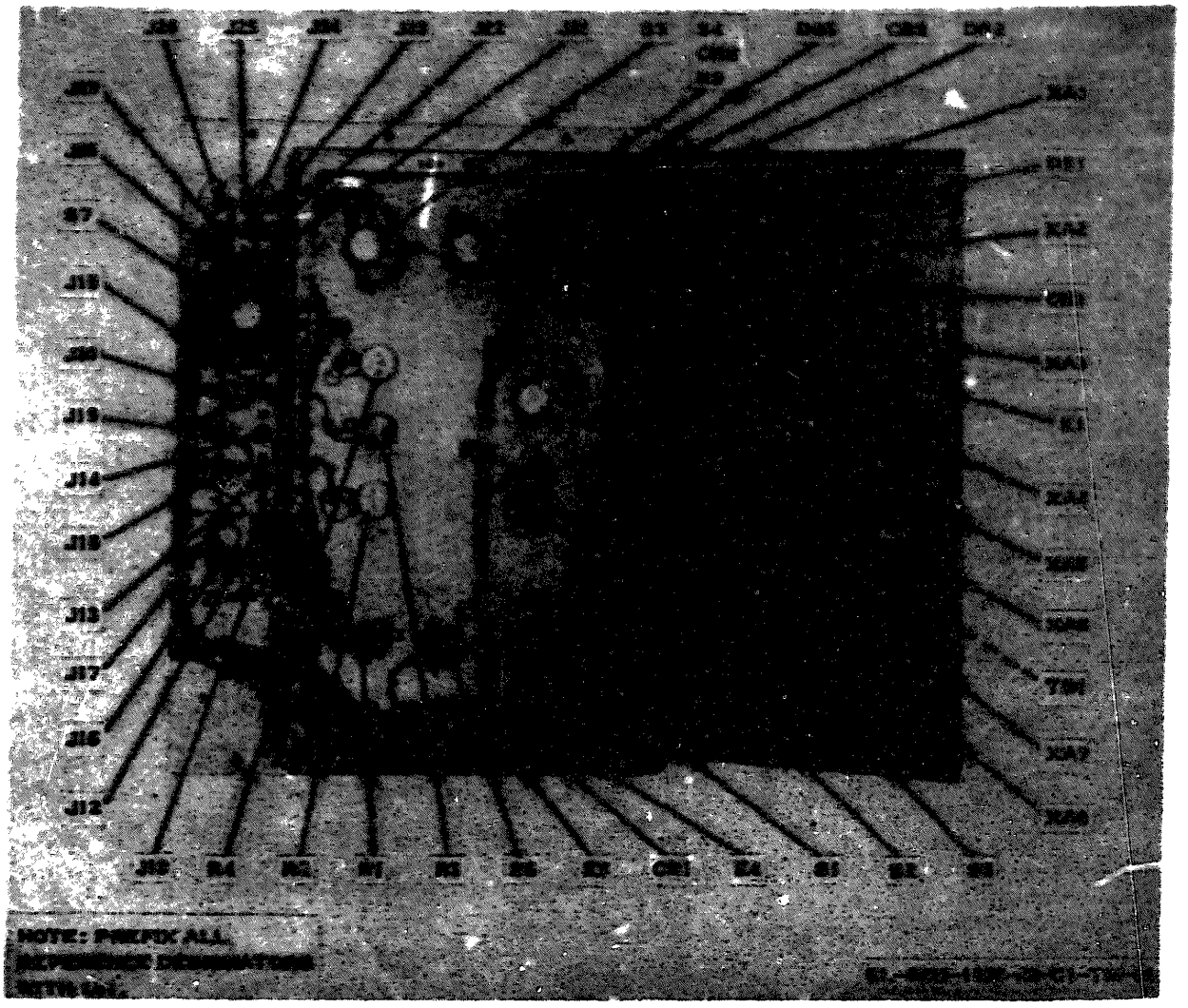

Figure 3-3(1). Parts location, control unit 1A1 (part 1 of 2).

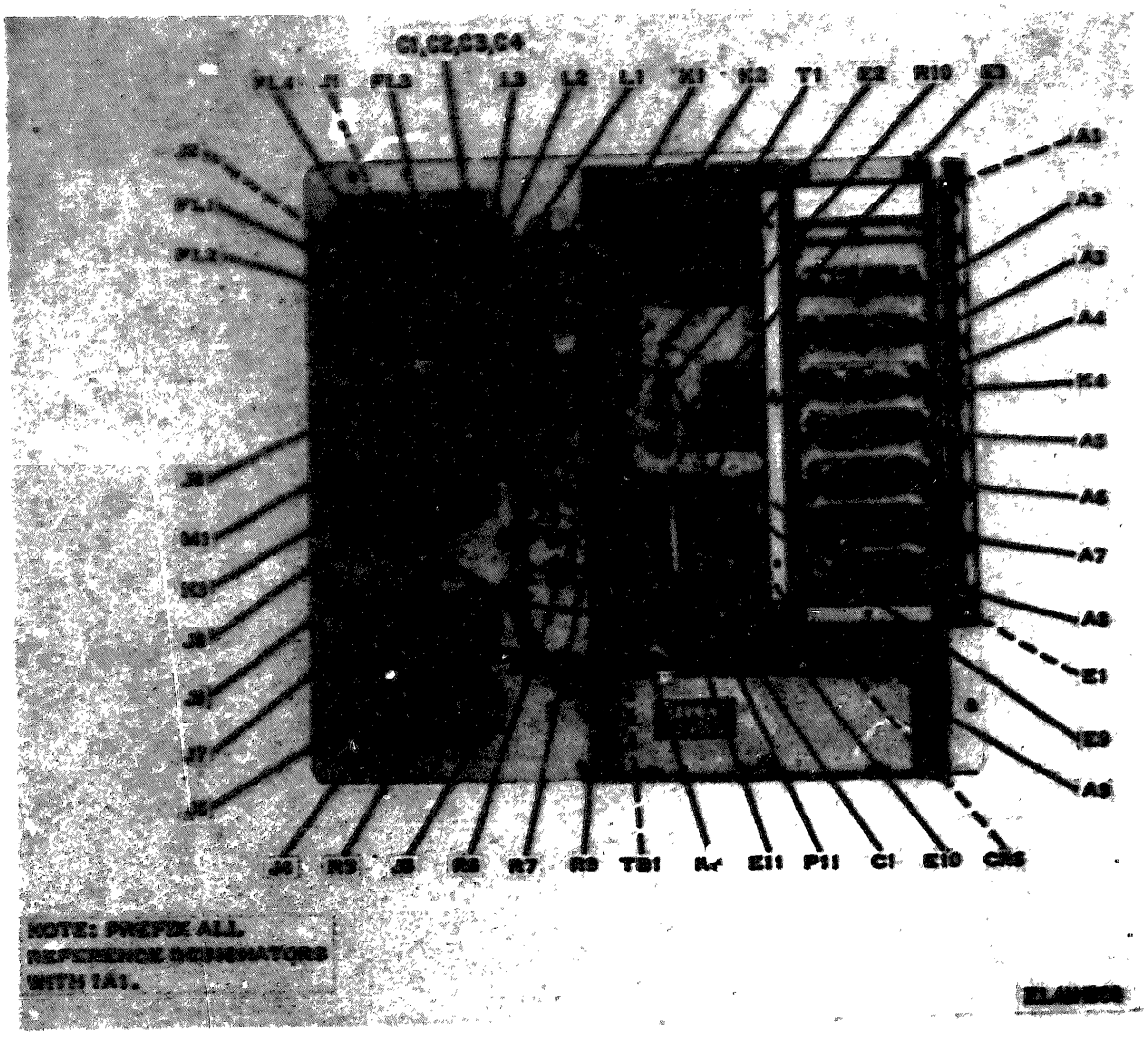

Figure 3-3(2). Parts location, control unit 1A1 (part 2 of 2).

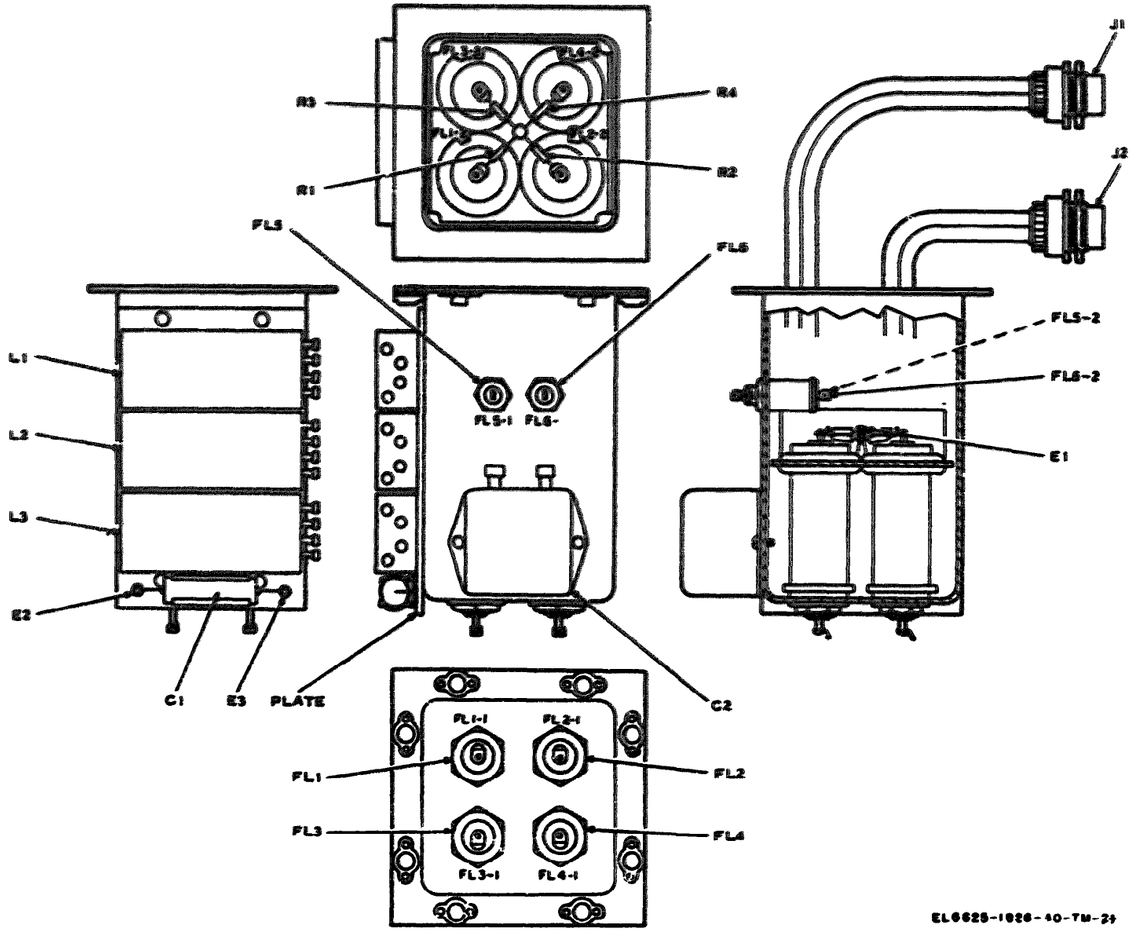

Figure 3-4. Parts location, filter assembly 1A1A10.

Section IV. Adjustment and Alignment

3-9. Adjustment Procedures

a. Initial Preparation.

(1) Perform removal procedure (para 3-7) to remove control unit 1A1 from the carrying case and expose the printed circuit boards.

(2) Use extender boards obtained from the electronic maintenance kit as necessary for gaining access to board test points and variable resistors.

(3) Perform the preparation for use and the preliminary starting procedure as outlined in TM 11-6625-1826-12.

(4) Remove power from the indicator test set any time you are removing or replacing boards or extender boards.

(5) Exercise caution as terminals with voltage are exposed during this procedure.

(6) Perform preparation for use procedures as outlined in paragraph 3-3.

b. Test Equipment.

(1) Oscilloscope AN/USM-281A.

(2) Digital Voltmeter, Nonlinear Systems Model X-2.

c. Adjustments.

(1) Locate 15 vdc power supply board 1A1A5 (fig. 3-3③).

(2) Set TEST POINTS switch 1A1S7 to 1.

(3) Connect dvm HI to TEST POINTS 2 and LO to TEST POINTS 8.

(4) Adjust 1A1A5R12 for 15 ±0.3 vdc.

(5) Locate −15 vdc power supply board 1A1A6 (fig. 3-3②).

(6) Disconnect dvm HI and connect to TEST POINTS 3.

(7) Adjust 1A1A6R12 for −15 ±0.3 vdc.

(8) Locate integrated circuit power supply, 1A1A7 (fig. 3-3②).

(9) Disconnect dvm HI and connect to TEST POINTS 4.

(10) Adjust 1A1A7R14 for 5.0 ± 1.0 vdc.

(11) Locate 150/250 vdc power supply 1A1A8 (fig. 3-3③).

(12) Disconnect dvm HI and connect to TEST POINTS 1.

(13) Adjust 1A1A8R20 for 150 ±3.0 vdc disconnect and remove dvm.

(14) Locate miscellaneous circuits 1A1A3 (fig. 3-3③).

(15) Set TEST POINTS switch 1A1S7 to 4.

(16) Connect oscilloscope to SCOPE.

(17) Adjust 1A1A3R28 for +5 v amplitude.

(18) Set TEST POINTS switch 1A1S7 to 6.

(19) Adjust 1A1A3R19 for a pulse width of 2.2 ± 0.1 milliseconds.

(20) Set TEST POINTS switch 1A1S7 to 2.

(21) Adjust 1A1A3R30 for +2 volts and −2 volts amplitude.

(22) Adjust 1A1A3R44 for a 0.0 ± 0.3 vdc offset.

(23) Move oscilloscope probe to J7-i.

(24) Adjust 1A1A3R18 for 20-microsecond pulse width.

(25) Disconnect test equipment and return control unit 1A1 (para 3-8) to the carrying case.

3-10. Alignment

Alignment procedures are not required.

Section V. Repairs

3-11. Parts replacement Techniques

All parts are easily accessible and can be replaced without special procedures. The following general precautions apply to the equipment:

a. Use a pencil-type soldering iron with a 55-watt maximum capacity to prevent damage to transistors and similar components. If the iron is to be used with alternating current, use an isolating transformer between the soldering iron and the line. Do not use a soldering gun; damaging voltages can be induced in components.

b. When soldering transistor or diode leads, solder quickly; whenever wiring permits, use a heat sink (such as long-nosed pliers) between the soldered joint and the transistor or diode.

Use approximately the same lead length and dress as used originally.

c. Wiring diagram information and cable diagrams in figures FO-9 and FO-10 should be referred to as required to insure correct part replacements.

3-12. Parts Substitution

Do not substitute parts indiscriminately. Substitute parts only when the trouble has been isolated to a specific stage and the defective part has been localized.

Section VI. GENERAL SUPPORT TEST PROCEDURES

3-13. Purpose and Instructions

a. Test procedures contained in this section are to be used for general support maintenance to determine the acceptability of repaired equipment. These procedures set forth specific requirements that repaired equipment must meet before it is returned to the using organization.

b. Perform each test in sequence; do not vary the sequence. For each step, perform all the actions required in the *Control settings* column; then perform each specific test procedure and verify it against the performance standard.

3-14. Test Equipment Required for Testing

All test equipment required to perform the testing procedures of this section is listed in table 3-1.

3-15. Test Procedure

General support test procedures are contained in chart 3-8.

Chart 3-3. General Support Test Procedure

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Unit under test		
1	Dvm		Prepare dvm for use.	Paragraph 3-3
2	Scope		Prepare scope for use.	Paragraph 3-3
3		POWER mode switch:OFF	Place jumper between TEST POINTS 6 and 7.	
4		PATTERN: 3 VIDEO SELECT: TD AMPLIFIER SIGNAL: INPUT FIELD OF VIEW: X1 28 VDC: ON 115 VAC 3φ: ON CAL IND CONTROLS INPUT: 4 TEST POINTS switch: 1 VIDEO INTENSITY: Fully cw RETICLE INTENSITY: Fully ccw BRIGHTNESS: Fully ccw CONTRAST: Fully ccw		
5			Connect cables W1 and W2 to ac and dc power source.	
6		POWER mode switch: STBY		STBY lamp lights. No other lamps light.
7		POWER mode switch: OPR		OPR lamp lights. STBY lamp extinguishes. No other lamp lights.
8	Dvm selector: volts		Perform voltage measurements in paragraph 3-5c(3); table 3-2, items 1 through 6.	Observe dvm indication.

Step No.	Control settings: Test equipment	Control settings: Unit under test	Test procedure	Performance standard
9	Dvm selector: KΩ	Power mode switch: OFF	Check resistance values, paragraph 3-5c(3); table 3-3, items 6 and 8 through 14.	Observe dvm indication.
10			Check continuity as in paragraph 3-5c(3); table 3-4, items 1 through 26.	Observe dvm indication.
11		TEST POINTS switch: 2 Power mode switch: OPR	Connect oscilloscope ground to control panel GND; probe to SCOPE.	Observe waveform A, figure 3-2.
12		TEST POINTS switch: 4	Move oscilloscope probe to J6-g.	Observe waveform A, figure 3-2.
			Move oscilloscope probe to SCOPE.	Observe waveform B, figure 3-2.
13		TEST POINTS switch: 5	Move oscilloscope probe to J5-U.	Observe waveform B, figure 3-2.
			Move oscilloscope probe to SCOPE.	Observe waveform C, figure 3-2.
14		TEST POINTS switch: 6	Move oscilloscope probe to J5-V.	Observe waveform C, figure 3-2.
		CAL IND CONTROLS: 3 or 4.	Move oscilloscope probe to SCOPE	Observe waveform D, figure 3-2.
			Move oscilloscope probe to J8-S.	Observe waveform D, figure 3-2.
15			Move oscilloscope probe to J7-i.	Observe waveform E, figure 3-2.
			Move oscilloscope probe to TEST POINTS HORIZ SYNC and J8-T.	Observe waveform E, figure 3-2.
16		VIDEO SELECT: TD PATTERN: 4 VIDEO INTENSITY: Fully cw	Move oscilloscope probe to INP VID.	Observe waveform F, figure 3-2.
			Move oscilloscope probe to J6-e.	Observe waveform F, figure 3-2.
17		CAL IND CONTROLS: 2	Move oscilloscope probe to J8-R.	Observe waveform F, figure 3-2.
18		CAL IND CONTROLS: 3	Move oscilloscope probe to J8-N.	Observe waveform F, figure 3-2.
19		CAL IND CONTROLS: 1	Move oscilloscope probe to J8-U.	Observe waveform F, figure 3-2.
20			Move oscilloscope probe to VERT SYNC.	Observe waveform G, figure 3-2.
			Move probe to J5-X *Note.* The remainer of these tests are accomplished with indicator test set removed from the case. Refer to paragraph 3-7, section III for removal procedure.	Observe waveform C, figure 3-2.
21		PATTERN: 3	Remove miscellaneous circuit board 1A1A3. Move oscilloscope probe to XA3-6.	Observe waveform G, figure 3-2.
22			Move oscilloscope probe to XA3-18.	Observe waveform H, figure 3-2.

Step No.	Control settings: Test equipment	Control settings: Unit under test	Test procedure	Performance standard
23			Move oscilloscope probe to XA3-3. Replace miscellaneous circuit board 1A1A3.	Observe waveform I, figure 3-2.
24		PATTERN: 5 VIDEO INTENSITY: Fully cw	Remove video processor 1A1A2. Move oscilloscope probe to XA2-22.	Observe waveform J, figure 3-2.
25		PATTERN: 4		Observe waveform M, figure 3-2 increases in amplitude.
26		PATTERN: 3		Observe waveform C, figure 3-2; 3.7±0.5 v p-p amplitude.
27		PATTERN: 2		Observe waveform K, figure 3-2.
28		PATTERN: 1		Observe waveform L, figure 3-2.
			Replace video generator circuit board 1A1A1.	
29			Remove phase A at source. Reapply removed phase. Set POWER mode switch to RESET, release.	FAIL lamp lights, OPR lamp extinguishes, STBY lamp lights. FAIL lamp extinguishes, STBY lamp extinguishes, OPR lamp lights.
30			Remove phase B at source, and follow test procedure as outlined in step 29 above.	
31			Remove phase C at source, and follow test procedure as outlined in step 29 above.	
32			Remove phases A and B at source. Plug A phase into B, and B phase into A. Reapply phases into appropriate positions. Set POWER mode switch to RESET, release.	FAIL lamp lights, OPR lamp extinguishes, STBY lamp lights. FAIL lamp extinguishes, STBY lamp extinguishes, OPR lamp lights.
33			Follow the procedure in step 32 for phases A and C.	
34			Follow the procedure in step 32 for phases B and C.	

APPENDIX

REFERENCES

The following publications contain information applicable to the general support maintenance of Test Set, Terrain-Calibration Indicator AN/AAM-33:

DA Pam 310-4	Index of Technical Manuals, Technical Bulletins, Supply Manuals (types 7, 8, and 9) Supply Bulletins and Lubrication Orders.
DA Pam 310-7	U. S. Army Equipment Index of Modification Work Orders.
TM 11-5850-241-34/1	DS and GS Maintenance Manual for Detecting Set, Infrared AN/AAS-24(U).
TM 11-5850-241-34/2(C)	DS and GS Maintenance Manual for Detecting Set, Infrared AN/AAS-24(U).
TM 11-6625-366-15	Organizational, DS, GS, and Depot Maintenance Manual for Multimeter TS-352B/U.
TM 11-6625-1703-15	Operator, Organizational, DS, GS, and Depot Maintenance Manual for Oscilloscope AN/USM-281A (Including Repair Parts and Special Tools Lists).
TM 11-6625-1732-12	Operator and Organizational Maintenance Manual Including Repair Parts and Special Tools Lists for Test Set, Resolution AN/AAM-30; Fixture, Alignment MX-8409/AAS-24; Cable Assembly Set, Electrical MX-8408/AAS-24; Maintenance Kit, Electronic Equipment MK-1172/AAS-24.
TM 11-6625-1826-12	Operator and Organizational Maintenance Manual Including Repair Parts and Special Tools Lists for Test Set, Terrain-Calibration Indicator AN/AAM-33.
TB SIG 222	Solder and Soldering (TO 31-3-64).

By Order of the Secretary of the Army:

W. C. WESTMORELAND,
General, United States Army,
Chief of Staff.

Official:

KENNETH G. WICKHAM,
Major General, United States Army,
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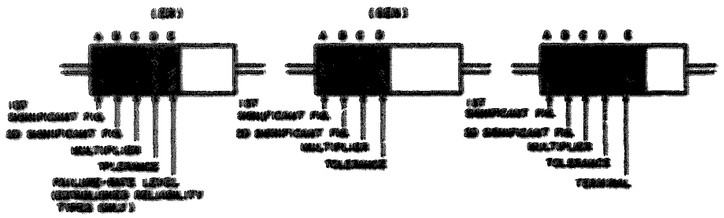


COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS.

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS.

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS.

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM.
BLACK	0	BLACK	0	BLACK	1			BROWN	M	
BROWN	1	BROWN	1	BROWN	10			RED	P	
RED	2	RED	2	RED	100			ORANGE	R	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP TYPE ONLY)	WHITE	-	SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE.

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL. ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL.

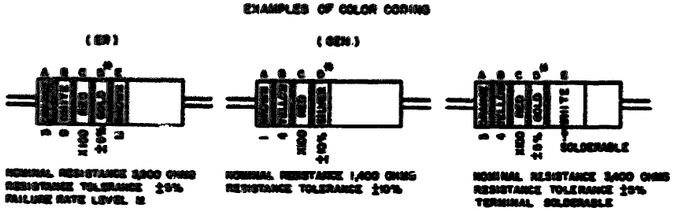
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS 1K0 = 1.0 K OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED, IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS.

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,900 OHMS
RESISTANCE TOLERANCE ±2%
FAILURE RATE LEVEL M

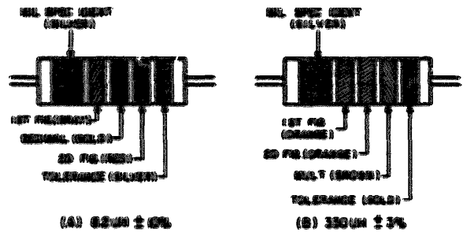
NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

NOMINAL RESISTANCE 3400 OHMS
RESISTANCE TOLERANCE ±2%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD.

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS.



COLOR CODING FOR TUBULAR ENCAPSULATED R.F CHOKES. AT A, AN EXAMPLE OF OF THE CODING FOR AN 0.82UH CHOKE IS GIVEN. AT B, THE COLOR BANDS FOR A 330UH INDUCTOR ARE ILLUSTRATED.

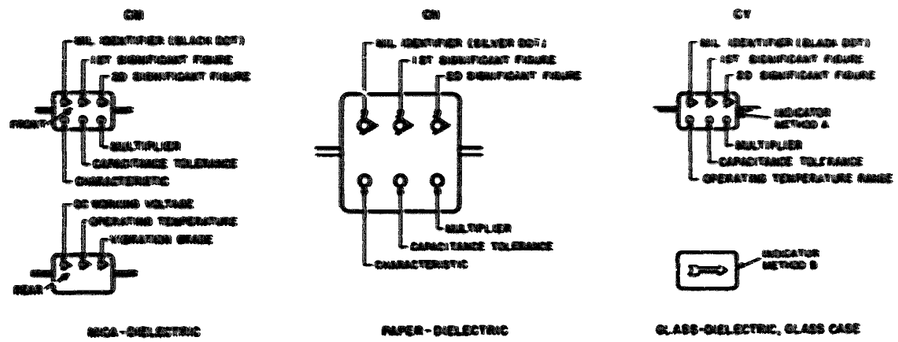
TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F CHOKES.

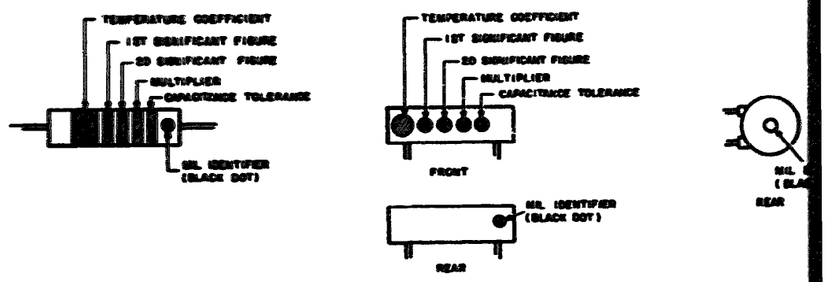
COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS.

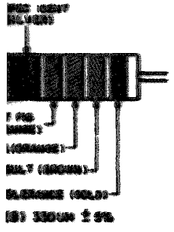
CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CV, AND CB.





C. COLOR CODE MA

FO-1. Color code for military standard resistors, inductors, and capacitors.



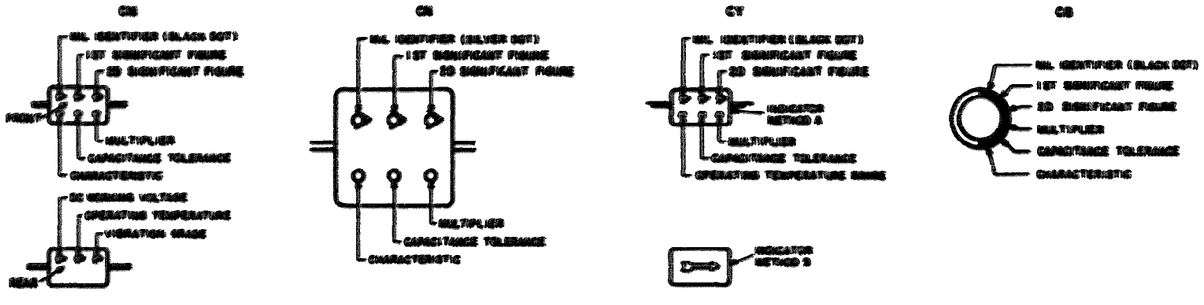
CHOKES. AT A, AN EXAMPLE OF AT B, THE COLOR BANDS FOR

COLOR	TOLERANCE (PERCENT)
	1
	2
	3
	20
	10
	5

E THE TWO COLOR FIGURES ISTANCE VALUE OF THE

BY STANDARD INDUCTORS.

CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB.



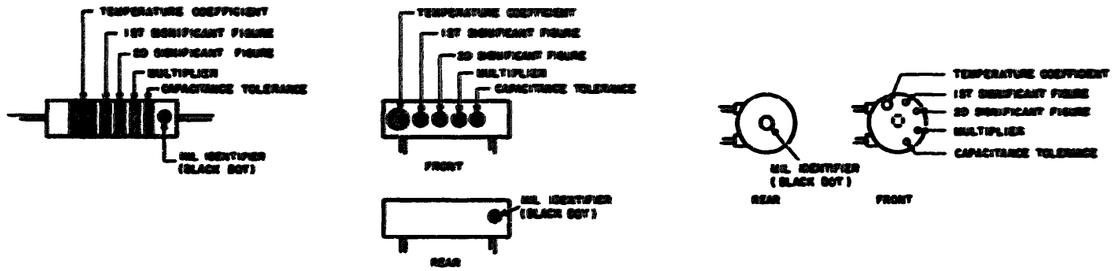


TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB.

COLOR	MIL ID	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER	CAPACITANCE TOLERANCE CM	CN	CY	CB	CHARACTERISTIC CM	CN	CB	DC WORKING VOLTAGE	OPERATING TEMP. RANGE CY, CN	VIBRATION GRADE CM
BLACK	SILVER DOT	0	0	1			±20%	±20%		A				
BROWN		1	1	10					B	C	D			
RED		2	2	100	±2%		±1%	±1%	C					
ORANGE		3	3	1,000		±30%			D		G	300		
YELLOW		4	4	10,000					E					
GREEN		5	5		±5%				F			500		
BLUE		6	6											
PURPLE (VIOLET)		7	7											
GREY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CM				±10%	±10%	±10%	±10%						

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC.

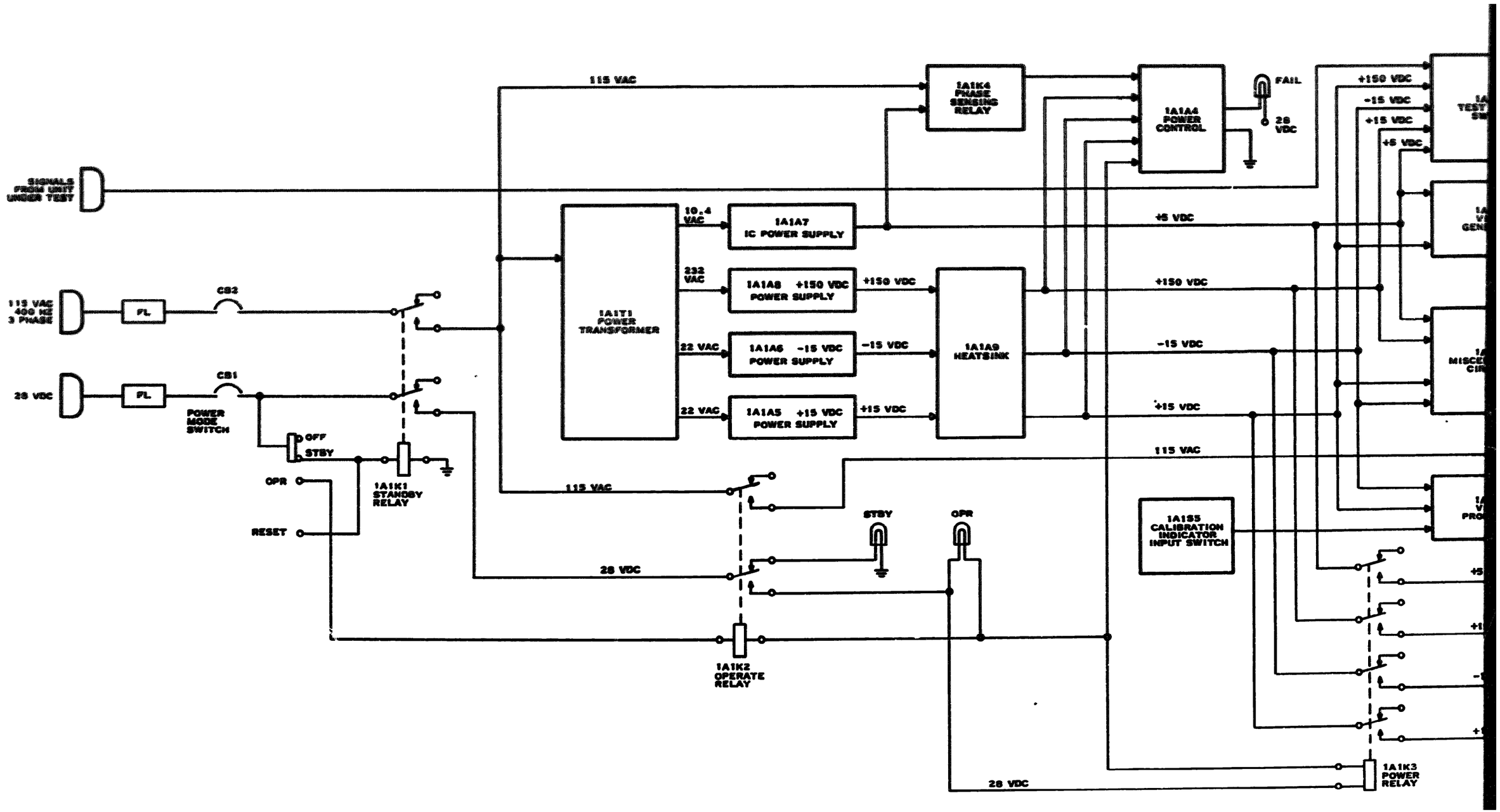
COLOR	TEMPERATURE COEFFICIENT[4]	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE: CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	MIL ID
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	−30	1	1	10	±1%		
RED	−80	2	2	100	±2%	±0.25 UUF	
ORANGE	−150	3	3	1,000			
YELLOW	−220	4	4				
GREEN	−330	5	5		±5%	±0.5 UUF	
BLUE	−470	6	6				
PURPLE (VIOLET)	−750	7	7				
GREY		8	8	0.01			
WHITE		9	9	0.1	±10%		
GOLD	+100					±1.0 UUF	
SILVER							

1. THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.
2. LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS: MIL-C-5, MIL-C-20, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.
3. LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015B.
4. TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE

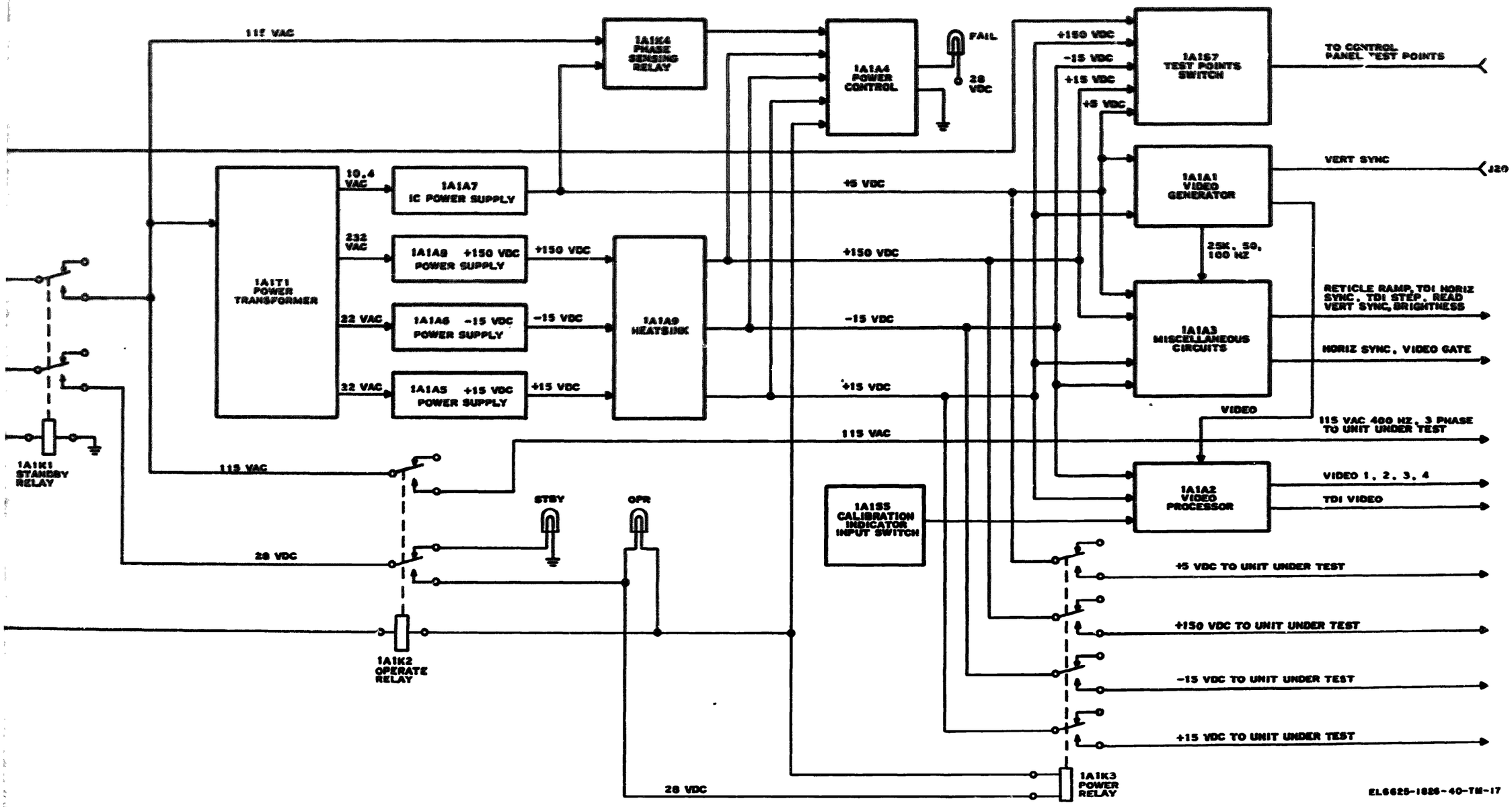
C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS.

ESC-7M 4113-60

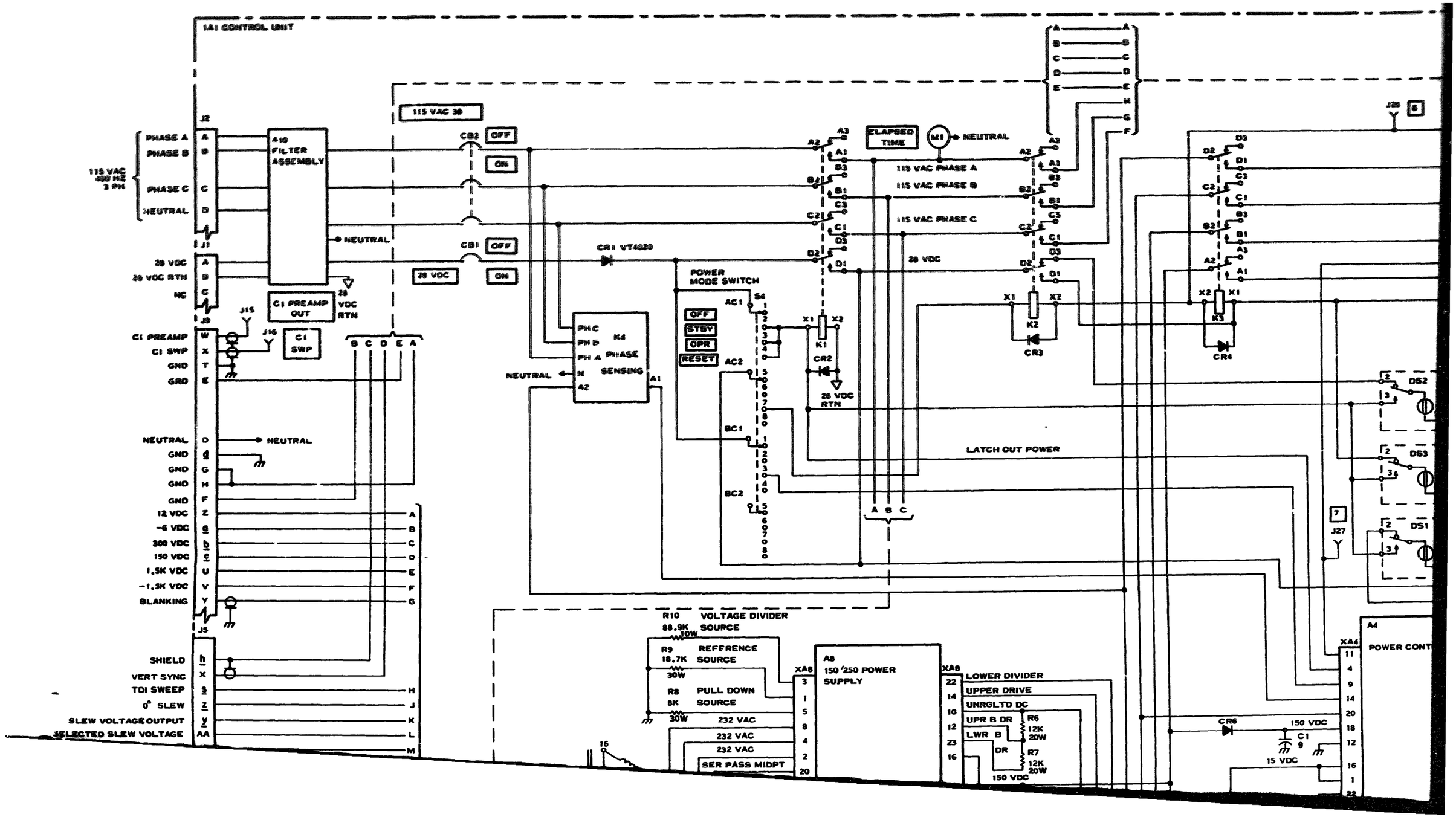
FO-1. Color code for military standard resistors, inductors, and capacitors.

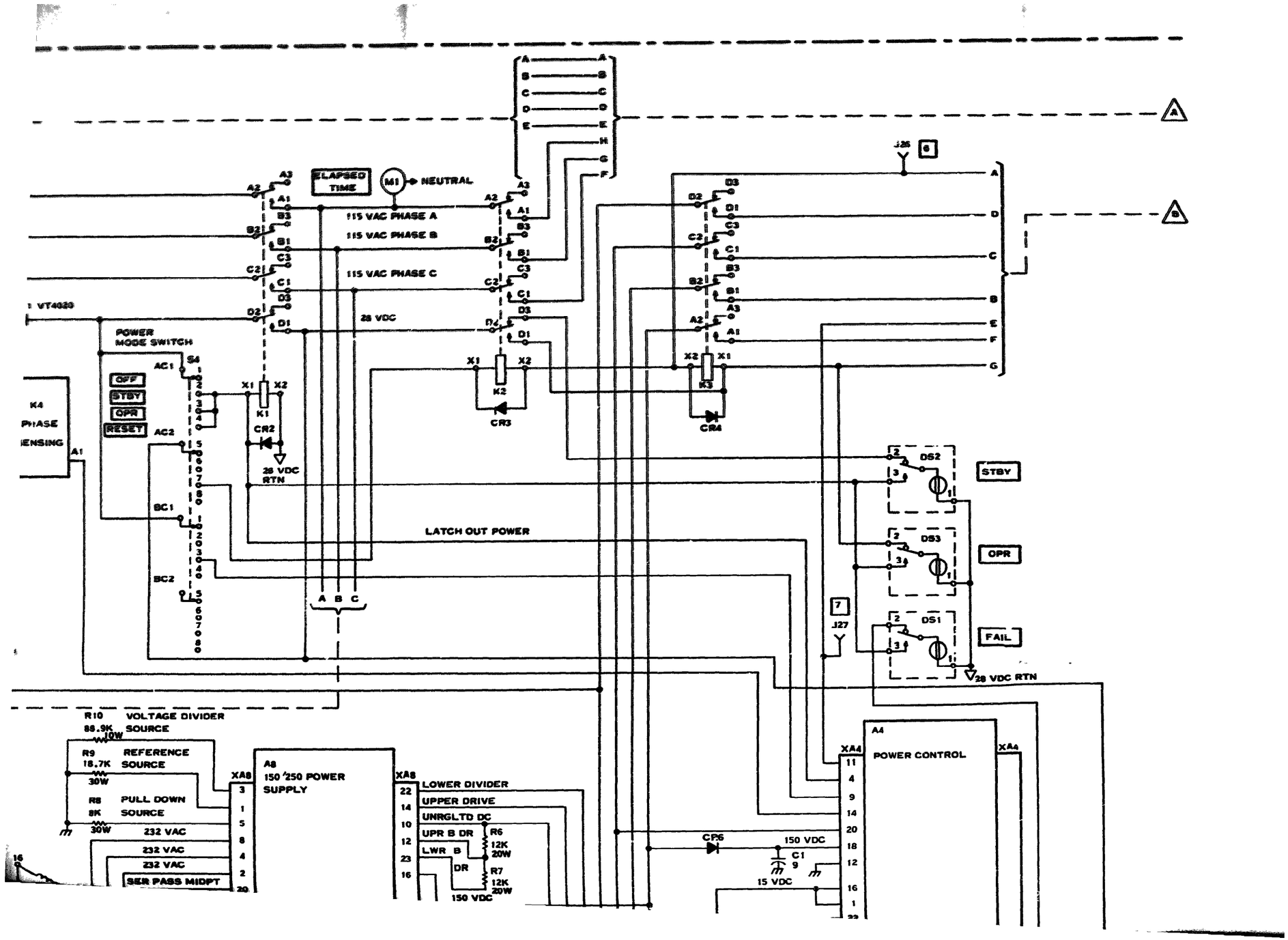


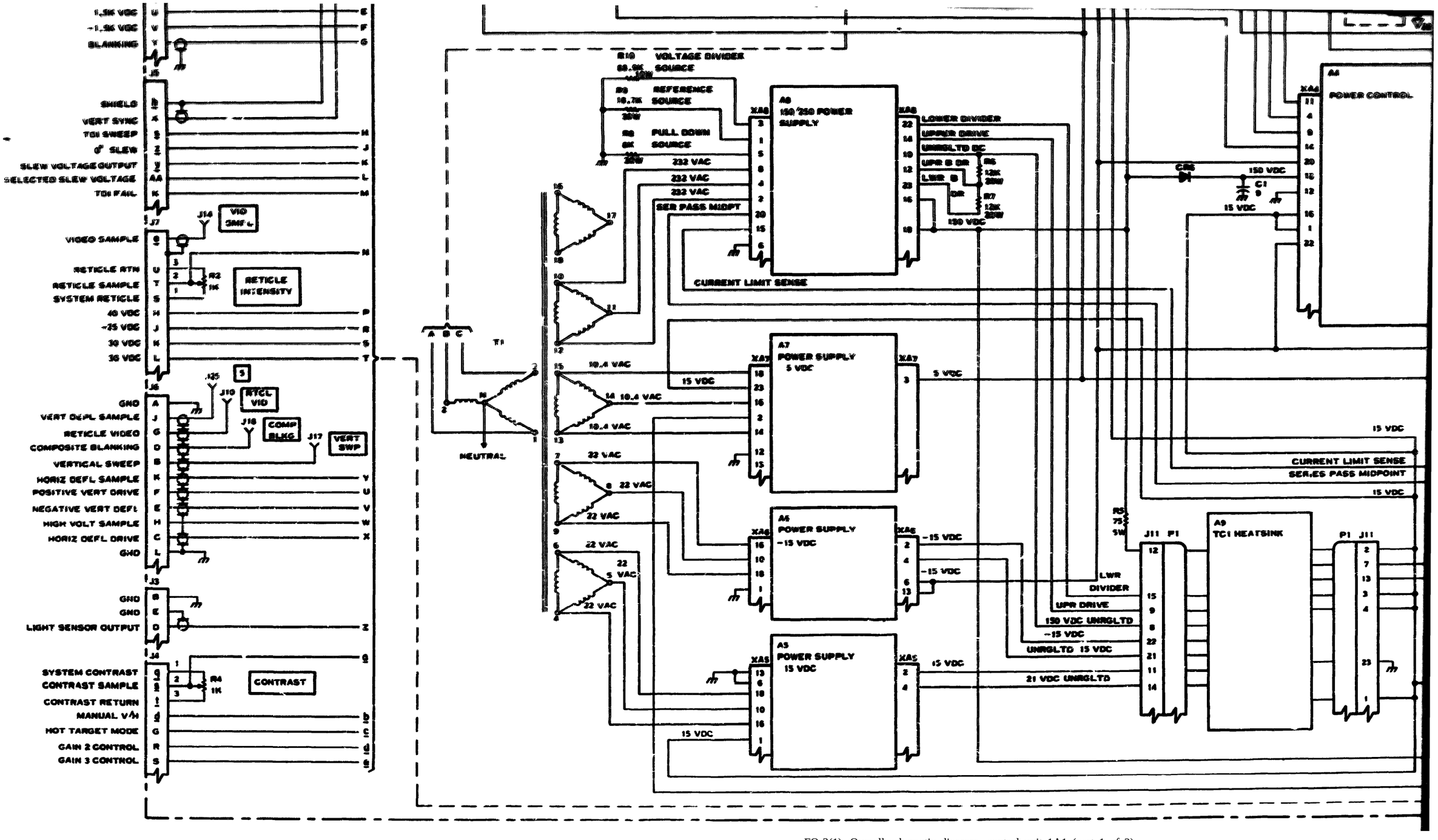
FO-2. Overall block diagram.



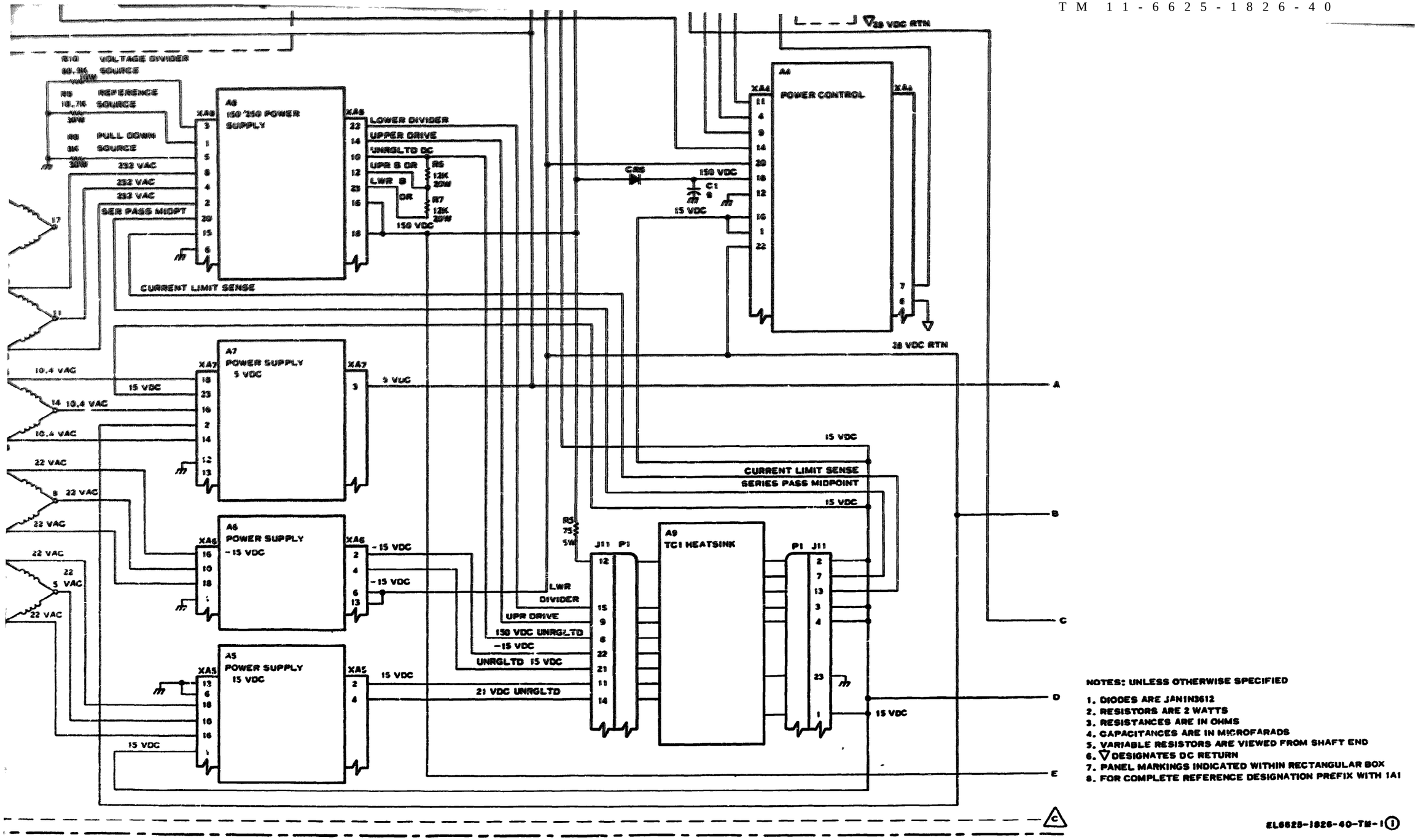
FO-2. Overall block diagram.


1A1 CONTROL UNIT
115 VAC 3Φ
J2
PHASE A
PHASE B
PHASE C
NEUTRAL
115 VAC 400 HZ 3 PH
A10 FILTER ASSEMBLY
CB2
CB1
OFF
ON
NEUTRAL
28 VDC
28 VDC RTN
NC
J1
J3
C1 PREAMP OUT
C1 PREAMP
C1 SWP
GND
GRD
J15
J16
C1 SWP
CR1 VT4020
PHC
PHB
PHA
N
A2
K4
PHASE SENSING
A1
POWER MODE SWITCH
OFF
STBY
OPR
RESET
AC1
AC2
BC1
BC2
S4
K1
K2
K3
CR2
CR3
CR4
ELAPSED TIME
M1
115 VAC PHASE A
115 VAC PHASE B
115 VAC PHASE C
28 VDC
28 VDC RTN
LATCH OUT POWER
A B C
J35
J27
DS1
DS2
DS3
NEUTRAL
GND
12 VDC
-6 VDC
300 VDC
150 VDC
1.5K VDC
-1.5K VDC
BLANKING
J5
SHIELD
VERT SYNC
TDI SWEEP
0° SLEW
SLEW VOLTAGE OUTPUT
SELECTED SLEW VOLTAGE
R10 VOLTAGE DIVIDER
88.9K SOURCE
10W
R9 REFFRENCE
18.7K SOURCE
30W
R8 PULL DOWN
8K SOURCE
30W
232 VAC
232 VAC
232 VAC
SER PASS MIDPT
A8
150/250 POWER SUPPLY
XA8
XA4
A4
POWER CONT
LOWER DIVIDER
UPPER DRIVE
UNRGLTD DC
UPR B DR
LWR B DR
R6 12K 20W
R7 12K 20W
150 VDC
CR6
C1
15 VDC


ELAPSED TIME
M1
NEUTRAL
115 VAC PHASE A
115 VAC PHASE B
115 VAC PHASE C
28 VDC
POWER MODE SWITCH
OFF
STBY
OPR
RESET
AC1
AC2
BC1
BC2
S4
K1
K2
K3
CR2
CR3
CR4
28 VDC RTN
LATCH OUT POWER
A B C
J25
J27
DS2
DS3
DS1
STBY
OPR
FAIL
R10 VOLTAGE DIVIDER
88.9K 10W SOURCE
R9 REFERENCE
18.7K 30W SOURCE
R8 PULL DOWN
8K 30W SOURCE
232 VAC
232 VAC
232 VAC
SER PASS MIDPT
A8
150 /250 POWER SUPPLY
XA8
LOWER DIVIDER
UPPER DRIVE
UNRGLTD DC
UPR B DR
LWR B DR
R6 12K 20W
R7 12K 20W
150 VDC
CR6
150 VDC
C1 9
15 VDC
A4
POWER CONTROL
XA4



FO-3(1). Overall schematic diagram, control unit 1A1 (part 1 of 2).

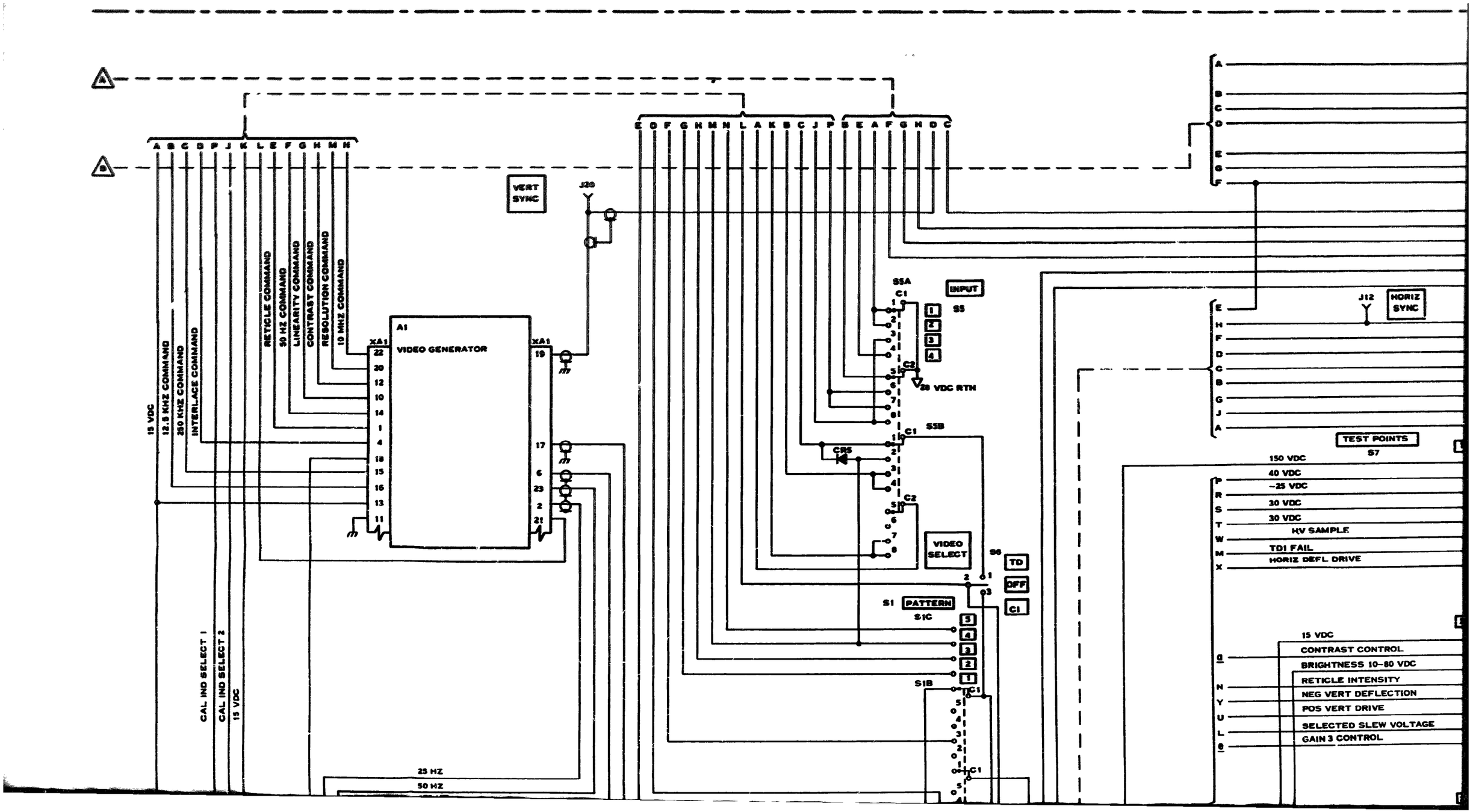


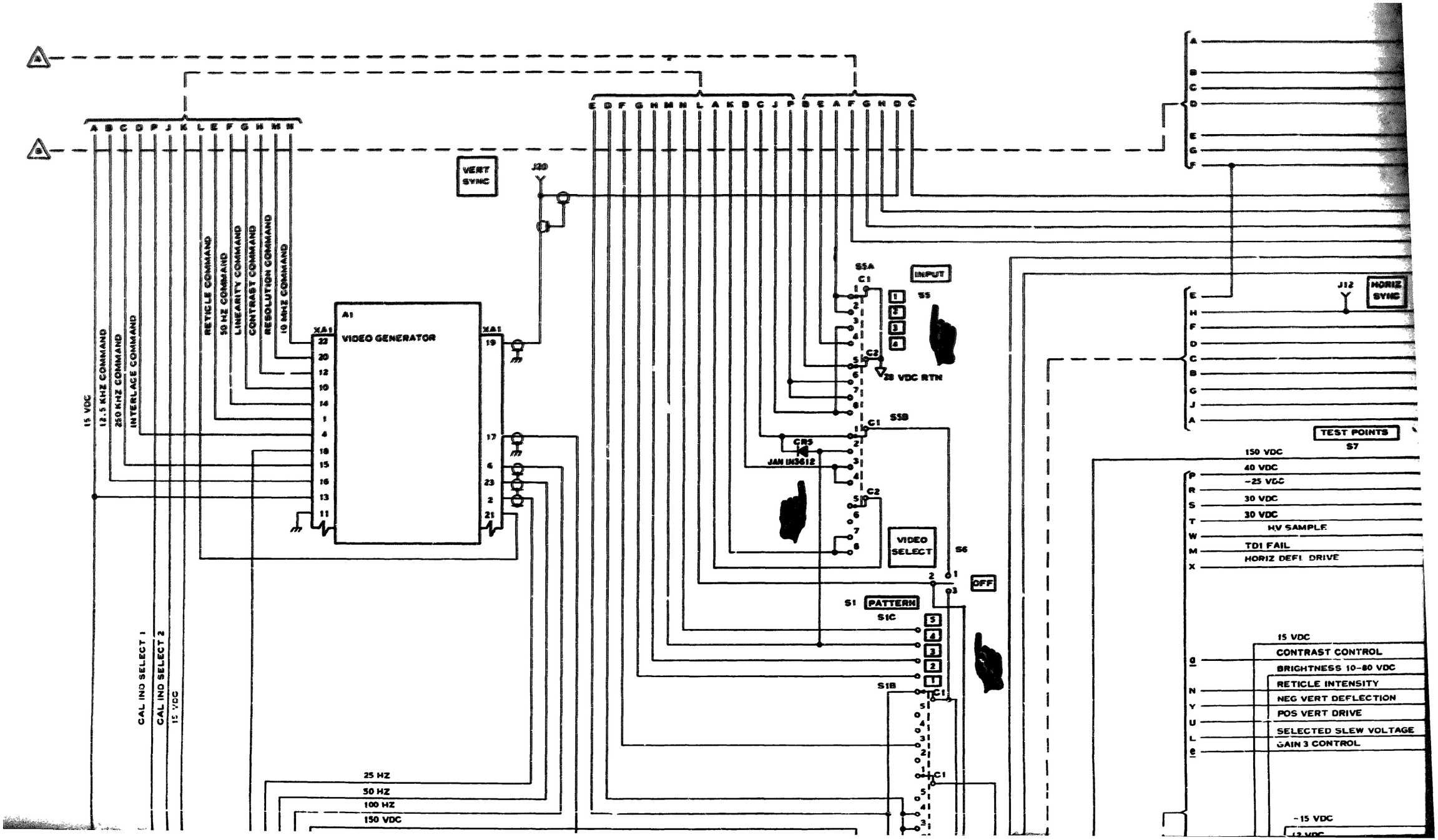
NOTES: UNLESS OTHERWISE SPECIFIED

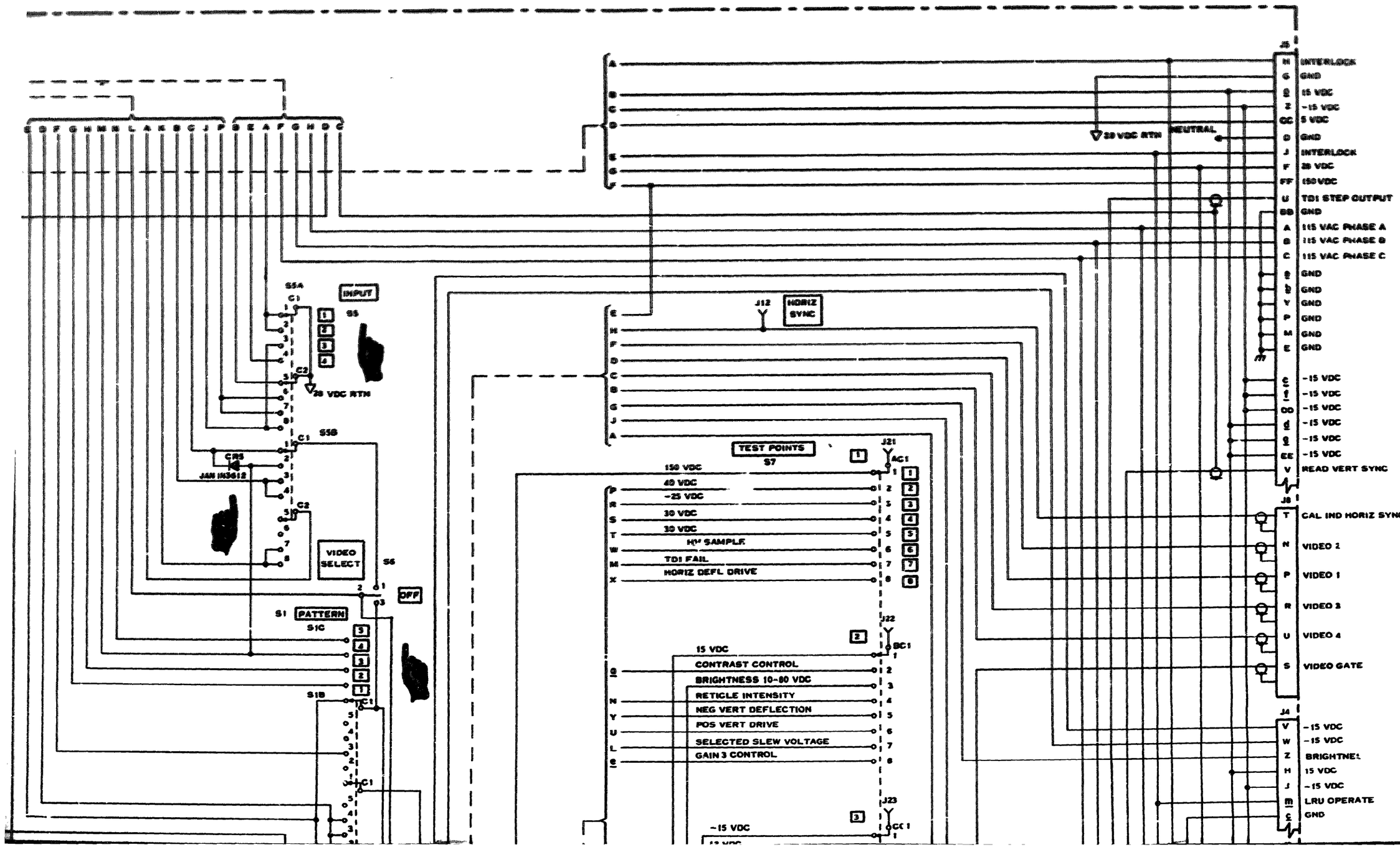
1. DIODES ARE JAN1N3612
2. RESISTORS ARE 2 WATTS
3. RESISTANCES ARE IN OHMS
4. CAPACITANCES ARE IN MICROFARADS
5. VARIABLE RESISTORS ARE VIEWED FROM SHAFT END
6. ▽ DESIGNATES DC RETURN
7. PANEL MARKINGS INDICATED WITHIN RECTANGULAR BOX
8. FOR COMPLETE REFERENCE DESIGNATION PREFIX WITH 1A1

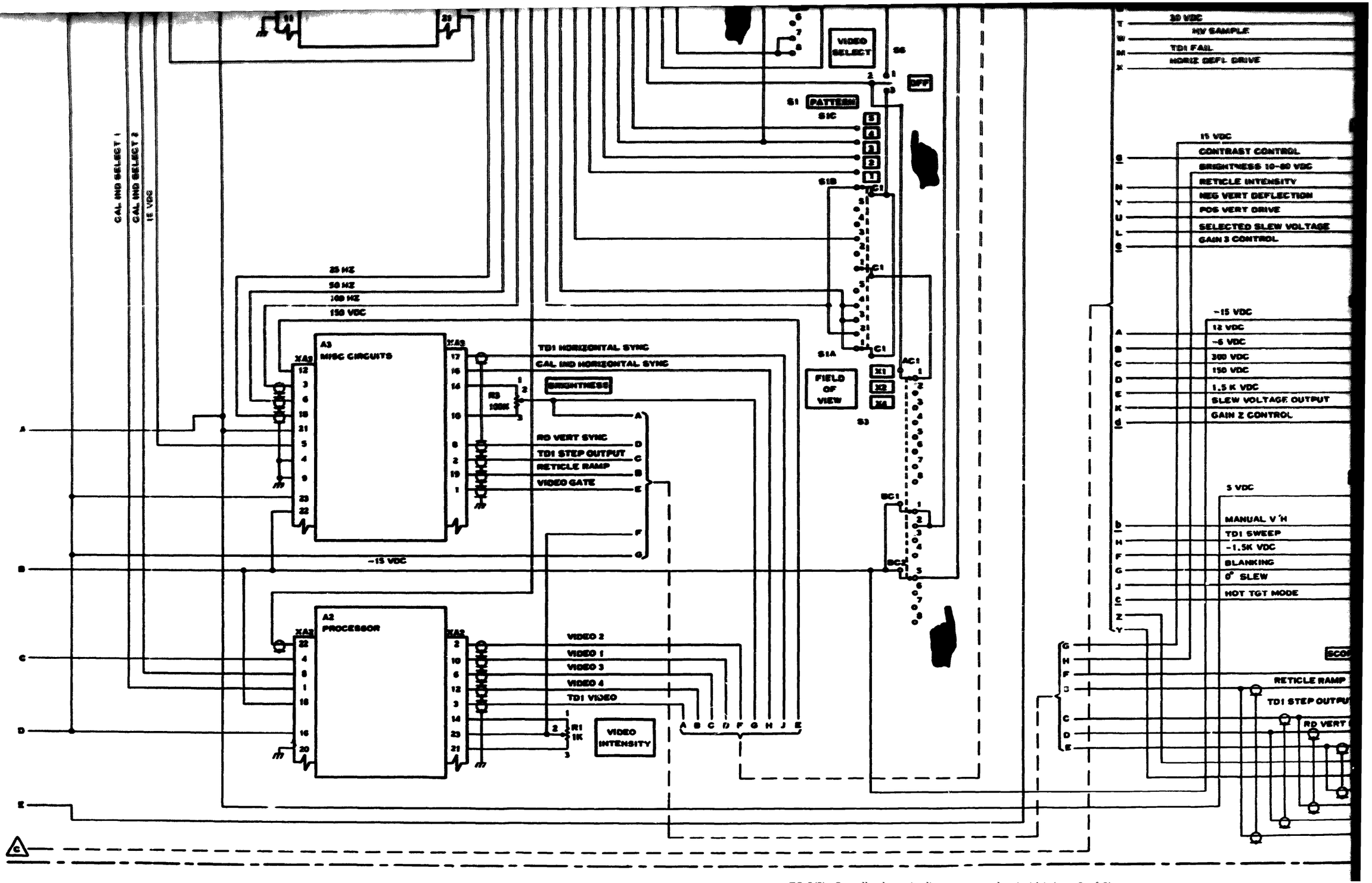
EL6625-1826-40-TM-1

FO-3(1). Overall schematic diagram, control unit 1A1 (part 1 of 2).

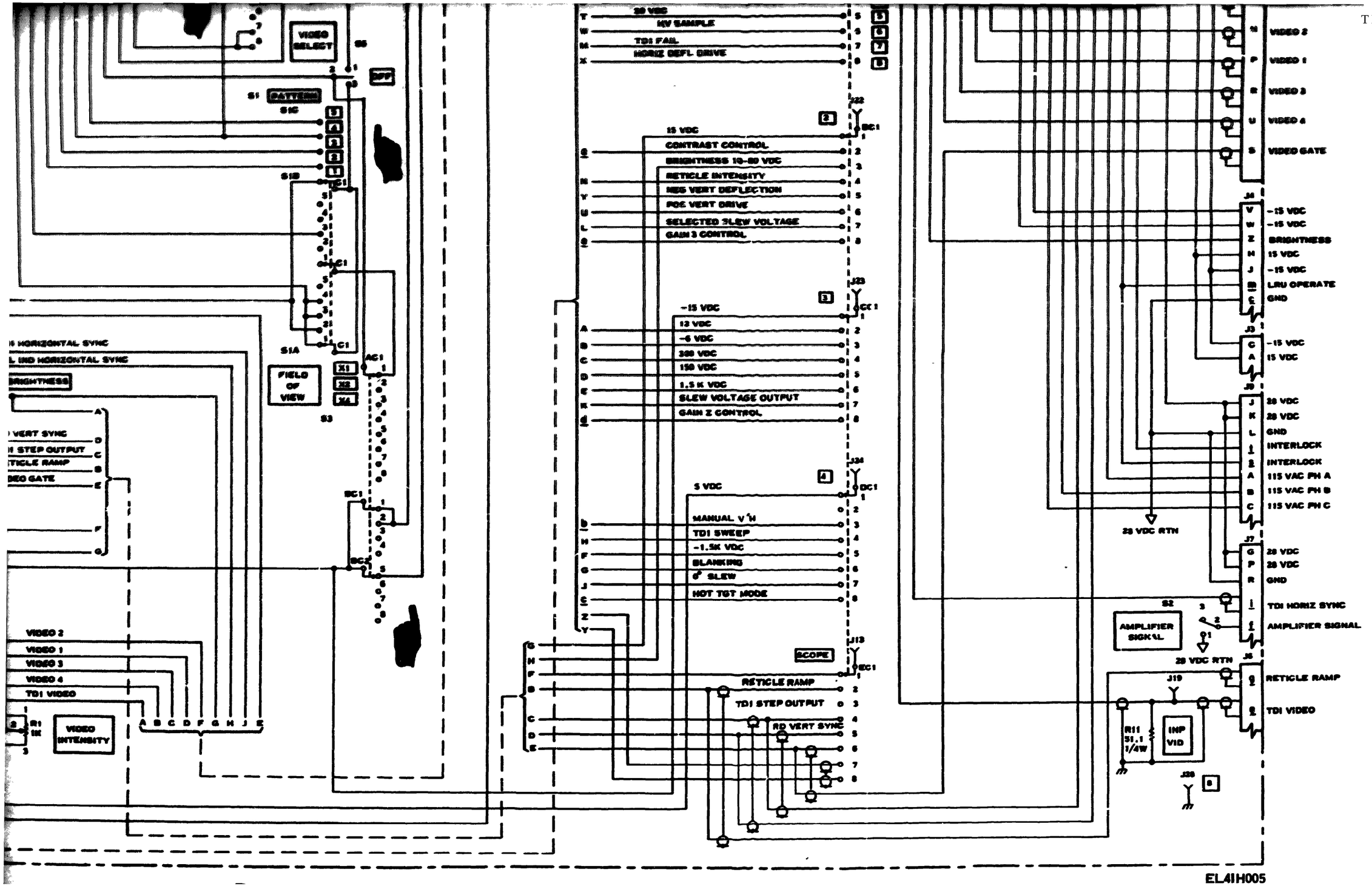

A1
VIDEO GENERATOR
XA1
XA1
VERT SYNC
J20
J12
HORIZ SYNC
15 VDC
12.5 KHZ COMMAND
250 KHZ COMMAND
INTERLACE COMMAND
RETICLE COMMAND
50 HZ COMMAND
LINEARITY COMMAND
CONTRAST COMMAND
RESOLUTION COMMAND
10 MHZ COMMAND
CAL IND SELECT 1
CAL IND SELECT 2
15 VDC
25 HZ
50 HZ
S5A
S5B
S5
INPUT
C1
C2
28 VDC RTN
CR5
S6
VIDEO SELECT
TD
OFF
C1
S1
PATTERN
S1C
S1B
S7
TEST POINTS
150 VDC
40 VDC
-25 VDC
30 VDC
30 VDC
HV SAMPLE
TDI FAIL
HORIZ DEFL DRIVE
15 VDC
CONTRAST CONTROL
BRIGHTNESS 10-80 VDC
RETICLE INTENSITY
NEG VERT DEFLECTION
POS VERT DRIVE
SELECTED SLEW VOLTAGE
GAIN 3 CONTROL


A
B
A B C D P J K L E F G H M N
15 VDC
12.5 KHZ COMMAND
250 KHZ COMMAND
INTERLACE COMMAND
RETICLE COMMAND
50 HZ COMMAND
LINEARITY COMMAND
CONTRAST COMMAND
RESOLUTION COMMAND
10 MHZ COMMAND
CAL IND SELECT 1
CAL IND SELECT 2
15 VDC
VERT SYNC
J20
A1
VIDEO GENERATOR
XA1
22
20
12
10
14
1
4
18
15
16
13
11
XA1
19
17
6
23
2
21
E D F G H M N L A K B C J P
B E A F G H D C
S5A
C1
C2
INPUT
S5
28 VDC RTN
S5B
CR5
JAN IN3612
VIDEO SELECT
S6
OFF
S1
PATTERN
S1C
S1B
25 HZ
50 HZ
100 HZ
150 VDC
A B C D E G F
E H F D C B G J A
J12
HORIZ SYNC
TEST POINTS
S7
150 VDC
40 VDC
-25 VDC
30 VDC
30 VDC
HV SAMPLE
TDI FAIL
HORIZ DEFL DRIVE
P R S T W M X
15 VDC
CONTRAST CONTROL
BRIGHTNESS 10-80 VDC
RETICLE INTENSITY
NEG VERT DEFLECTION
POS VERT DRIVE
SELECTED SLEW VOLTAGE
GAIN 3 CONTROL
Q N Y U L e
-15 VDC

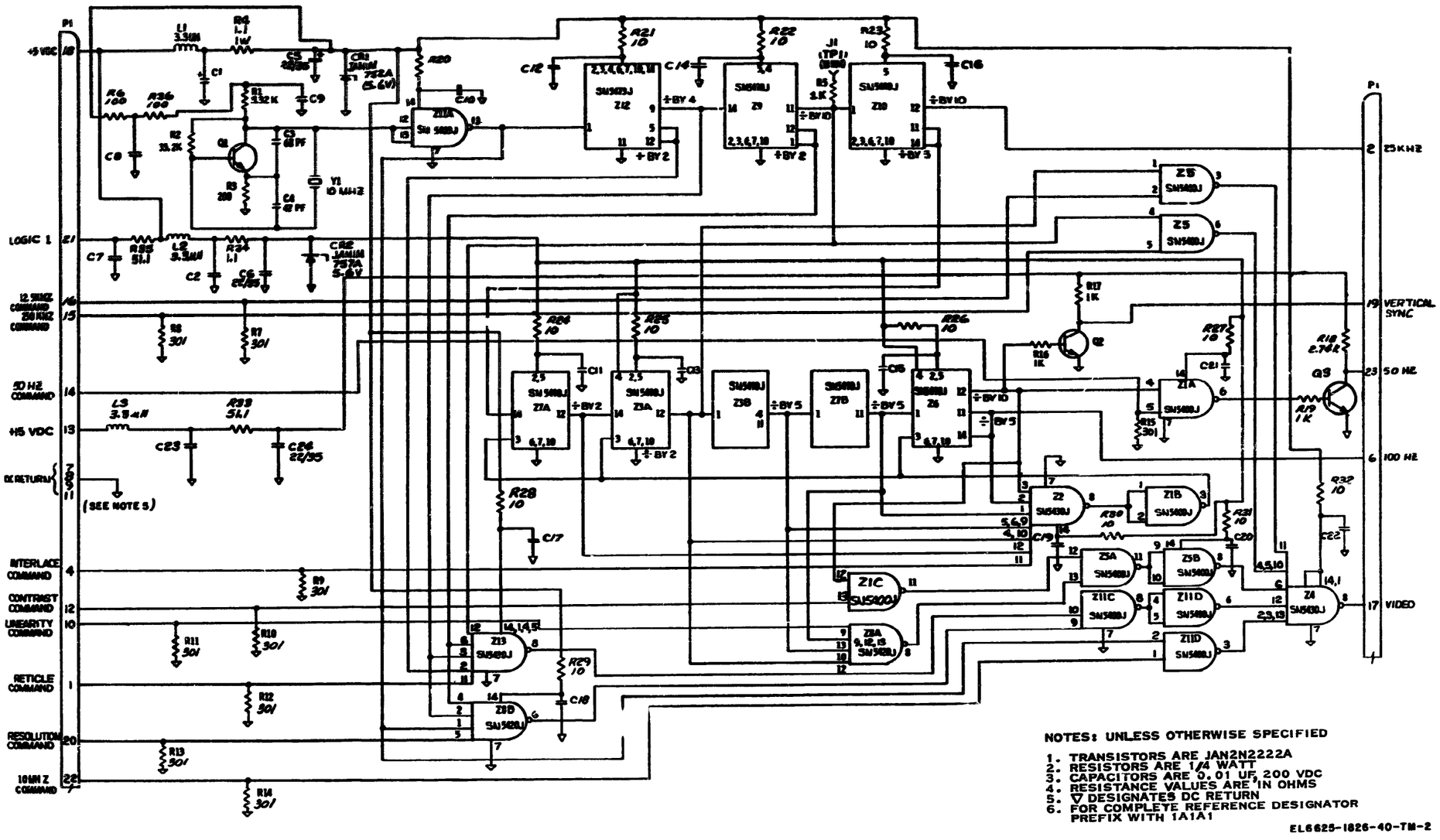

J5
N INTERLOCK
G GND
15 VDC
Z -15 VDC
CC 5 VDC
D GND
J INTERLOCK
F 28 VDC
FF 150 VDC
U TDI STEP OUTPUT
BB GND
A 115 VAC PHASE A
B 115 VAC PHASE B
C 115 VAC PHASE C
GND
GND
V GND
P GND
M GND
E GND
-15 VDC
-15 VDC
DD -15 VDC
-15 VDC
-15 VDC
EE -15 VDC
V READ VERT SYNC
J8
T CAL IND HORIZ SYNC
N VIDEO 2
P VIDEO 1
R VIDEO 3
U VIDEO 4
S VIDEO GATE
J4
V -15 VDC
W -15 VDC
Z BRIGHTNES
H 15 VDC
J -15 VDC
m LRU OPERATE
GND
28 VDC RTN
NEUTRAL
S5A
INPUT
S5
C2
28 VDC RTN
S5B
CR5
JAN IN3612
VIDEO SELECT
S6
OFF
S1 PATTERN
S1C
S1B
J12
HORIZ SYNC
TEST POINTS
S7
J21
150 VDC
40 VDC
-25 VDC
30 VDC
30 VDC
HV SAMPLE
TDI FAIL
HORIZ DEFL DRIVE
J22
15 VDC
CONTRAST CONTROL
BRIGHTNESS 10-80 VDC
RETICLE INTENSITY
NEG VERT DEFLECTION
POS VERT DRIVE
SELECTED SLEW VOLTAGE
GAIN 3 CONTROL
J23
-15 VDC



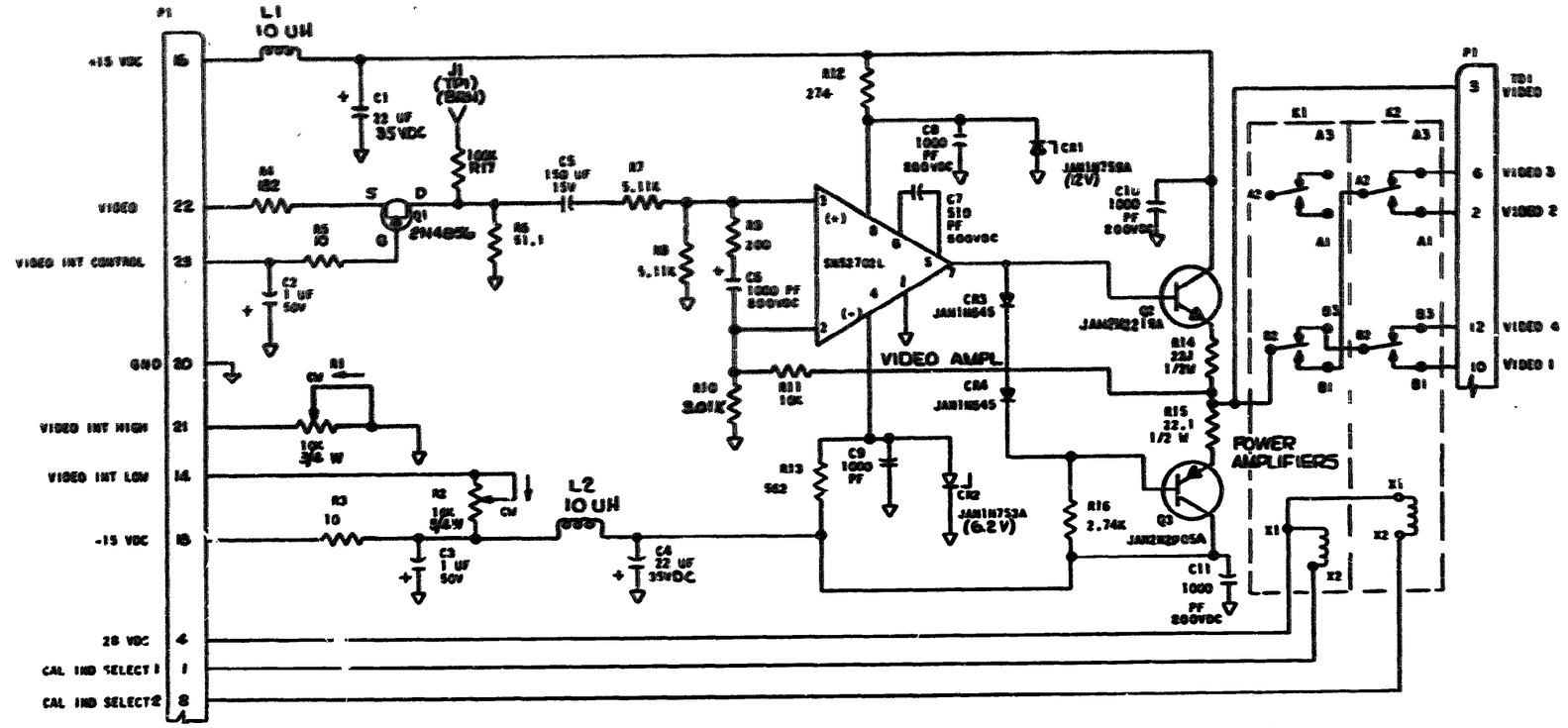
FO-3(3). Overall schematic diagram, control unit 1A1 (part 2 of 2).



FO-3(2). Overall schematic diagram, control unit 1A1 (part 2 of 2).



FO-4. Video generator 1A1A1, schematic.



Notes: Unless Otherwise Specified

1. Resistors are 1/4 watt
2. Resistance Values are in ohms
3. For complete reference designator prefix with 1A1A2

EL41H006

FO-5. Video processor 1A1A2, schematic diagram.

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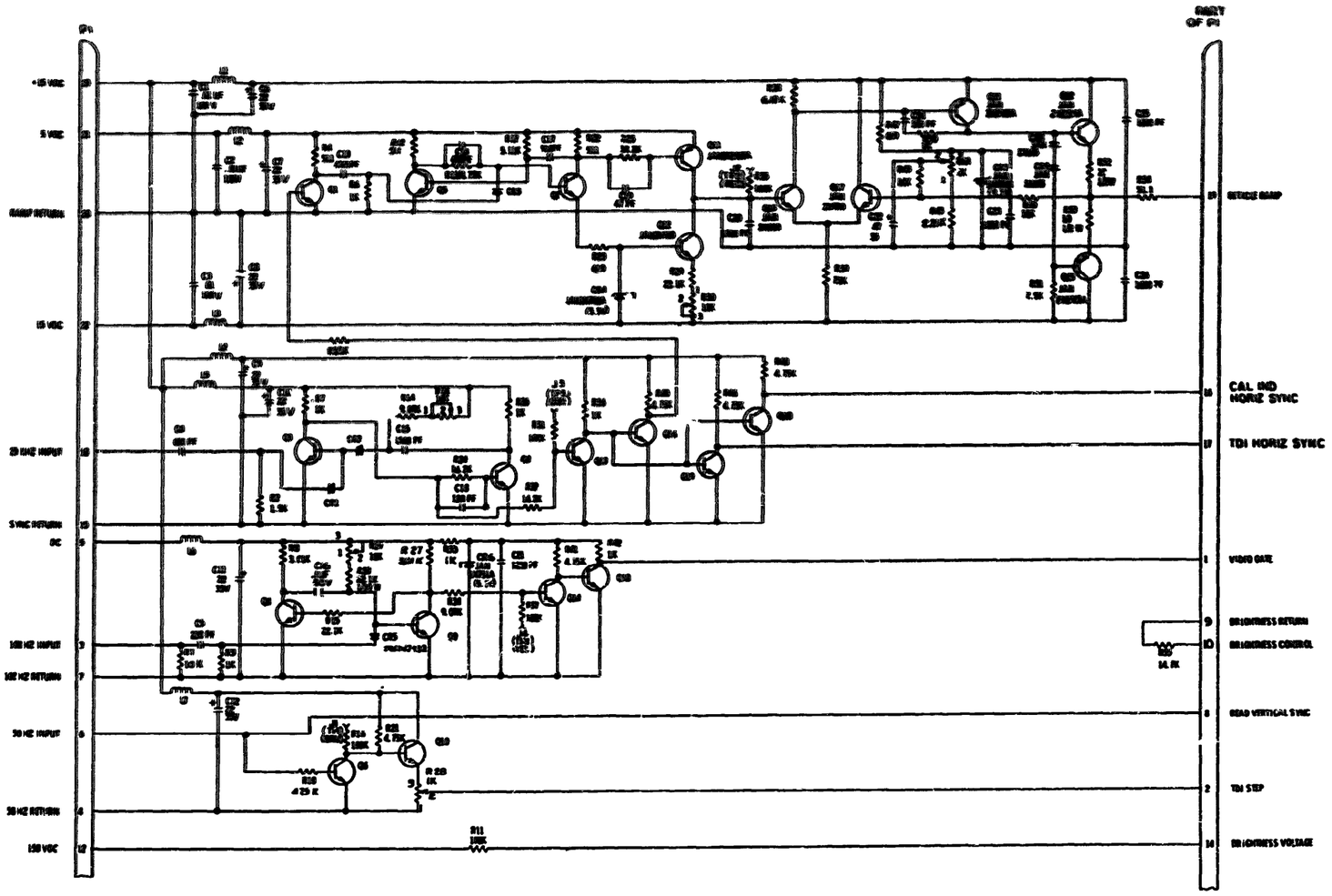
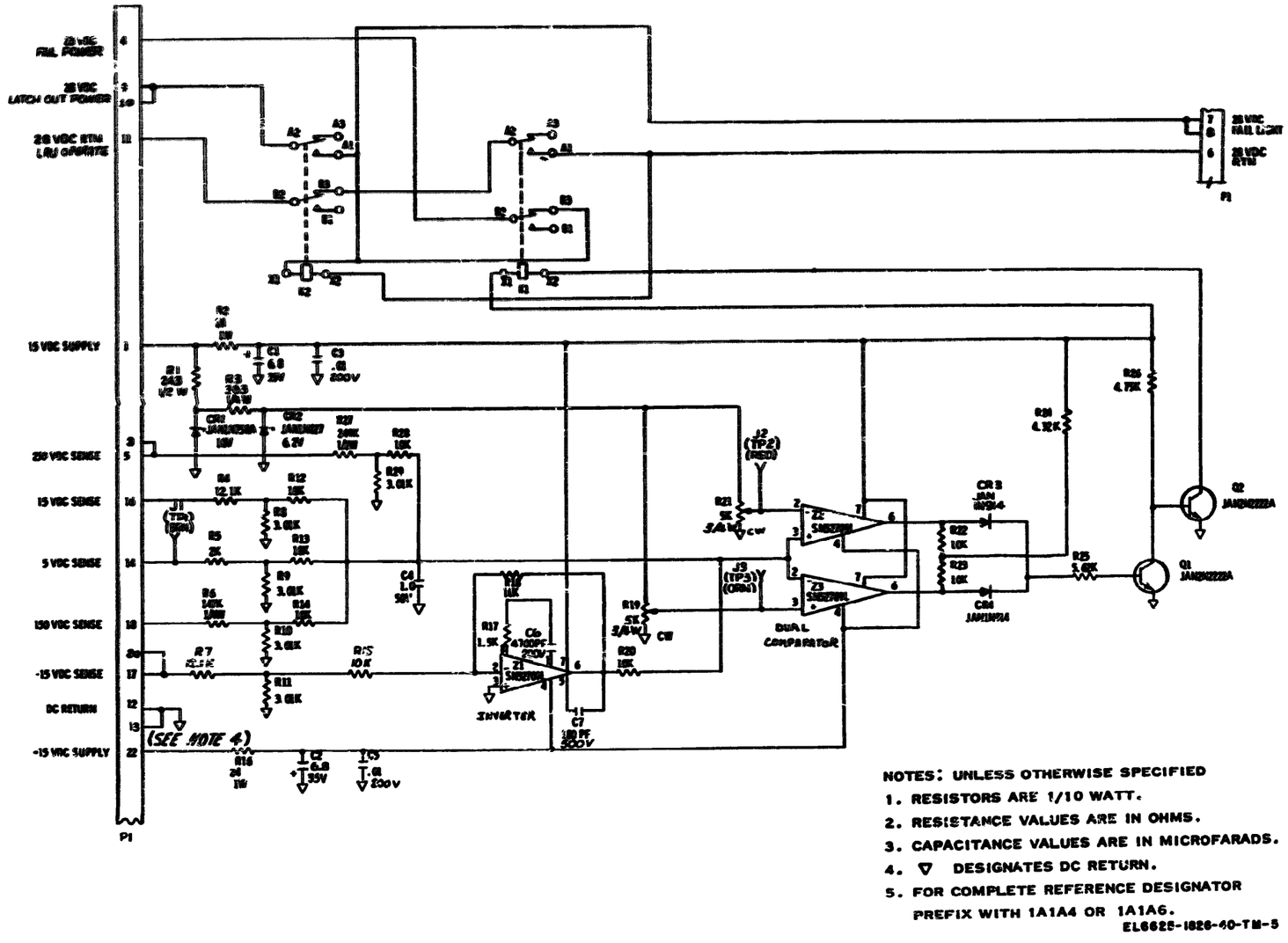


NOTES: UNLESS OTHERWISE SPECIFIED

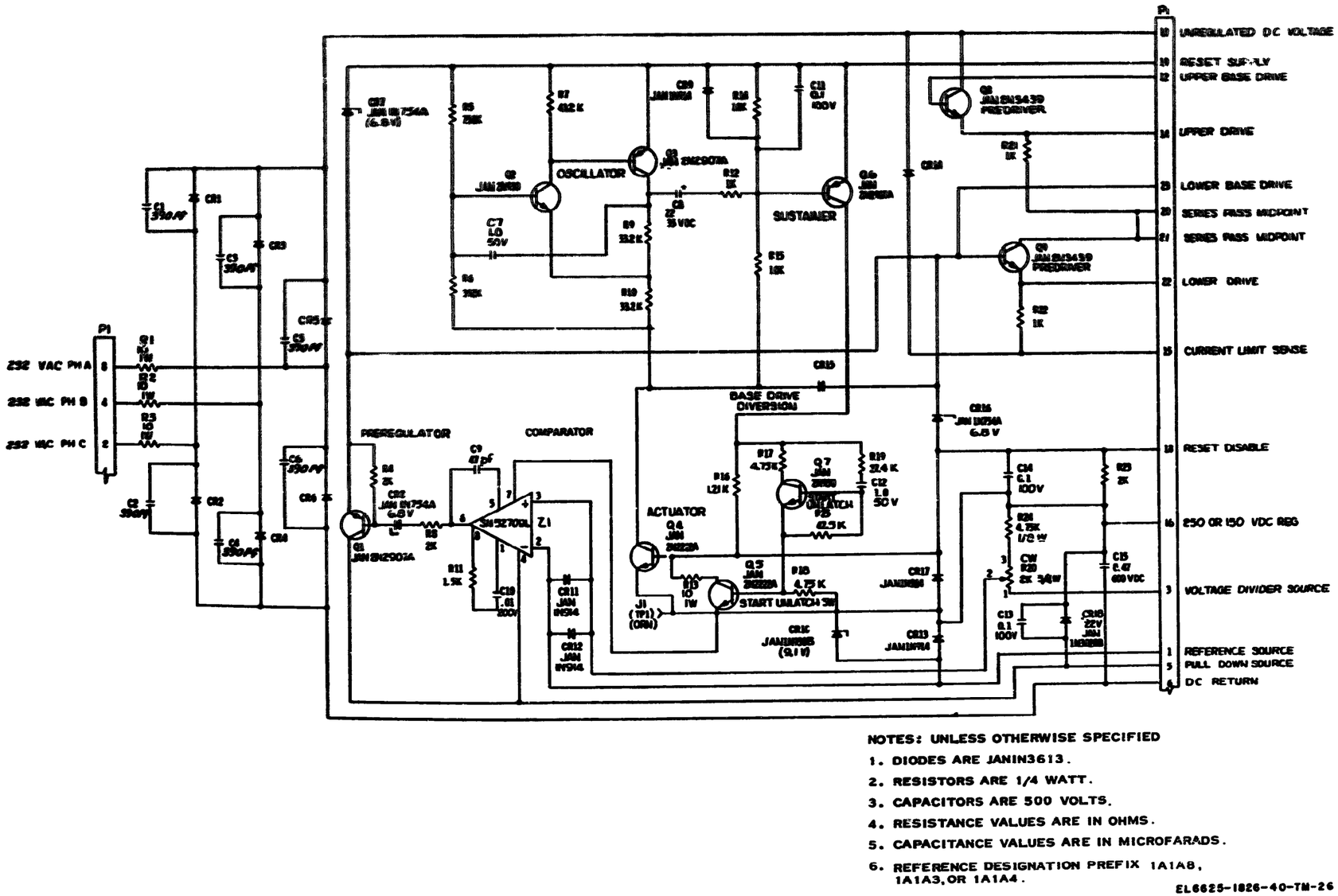
1. DIODES ARE JANIN914
2. TRANSISTORS ARE JAN2N2222A
3. RESISTORS ARE 1/4 WATT
4. ALL COILS ARE 10 UH
5. POTENTIOMETERS ARE 3/4 WATT
6. FOR COMPLETE REFERENCE DESIGNATOR PREFIX WITH 1A1A3

EL6625-1826-40-TM-4

FO-6. Miscellaneous circuits 1A1A3, schematic diagram.



FO-7. Power control 1A1A4, schematic diagram.



NOTES: UNLESS OTHERWISE SPECIFIED

1. DIODES ARE JANIN3613.
2. RESISTORS ARE 1/4 WATT.
3. CAPACITORS ARE 500 VOLTS.
4. RESISTANCE VALUES ARE IN OHMS.
5. CAPACITANCE VALUES ARE IN MICROFARADS.
6. REFERENCE DESIGNATION PREFIX 1A1A8, 1A1A3, OR 1A1A4.

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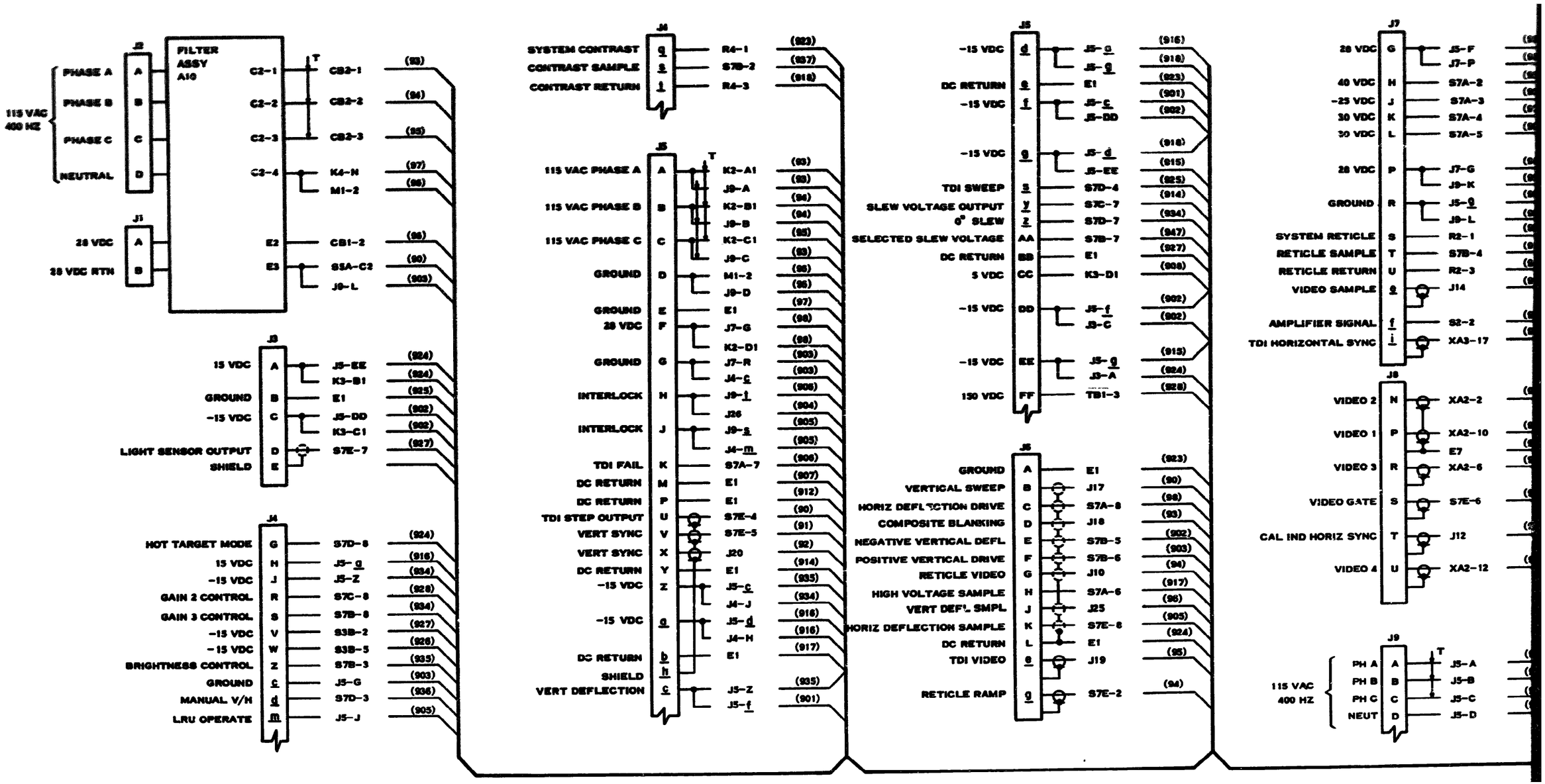
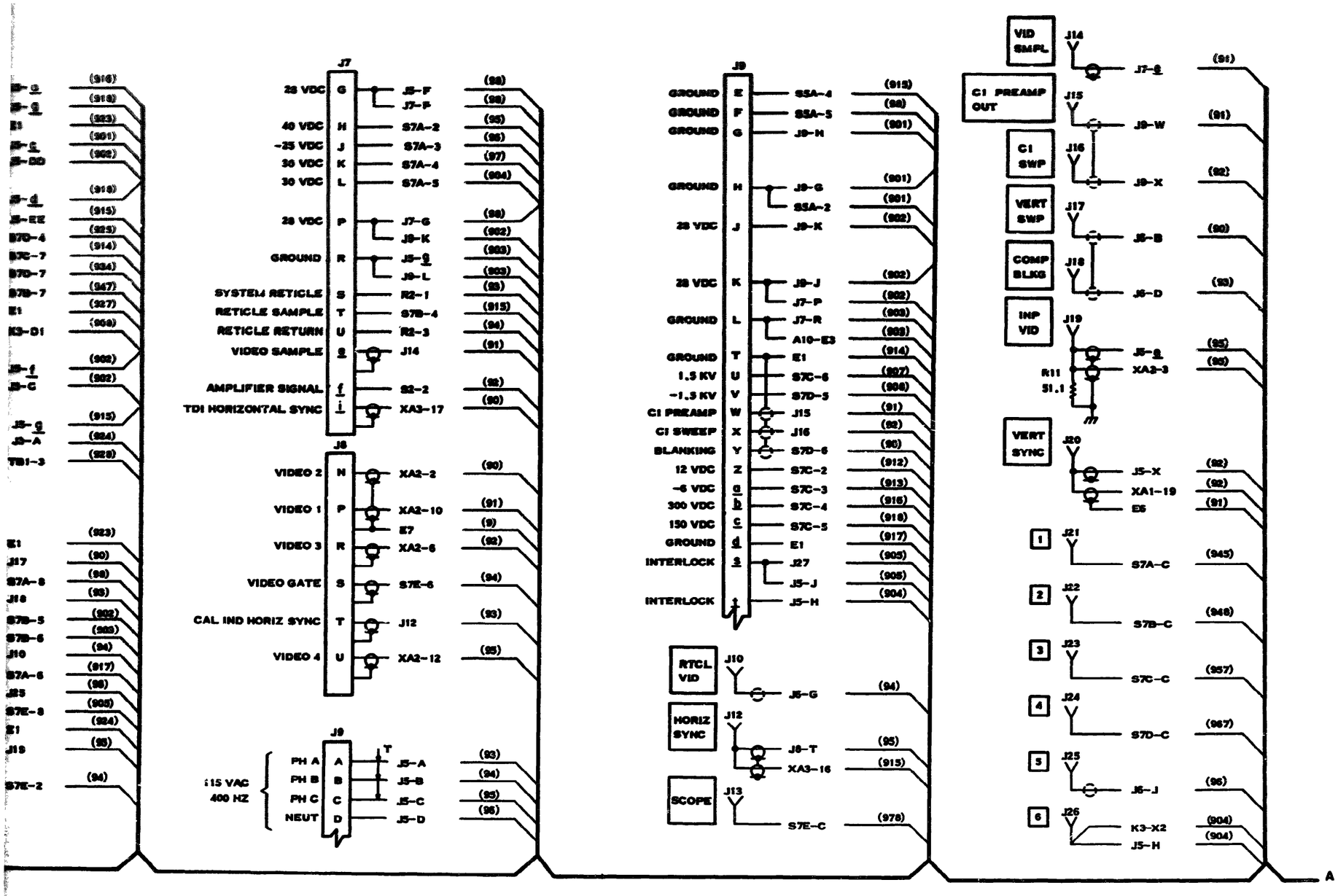
FO-8. 150/250-vdc power supply 1A1A8, schematic diagram



FO-9. Wiring diagram, control unit 1A1 (part 1 of 3).

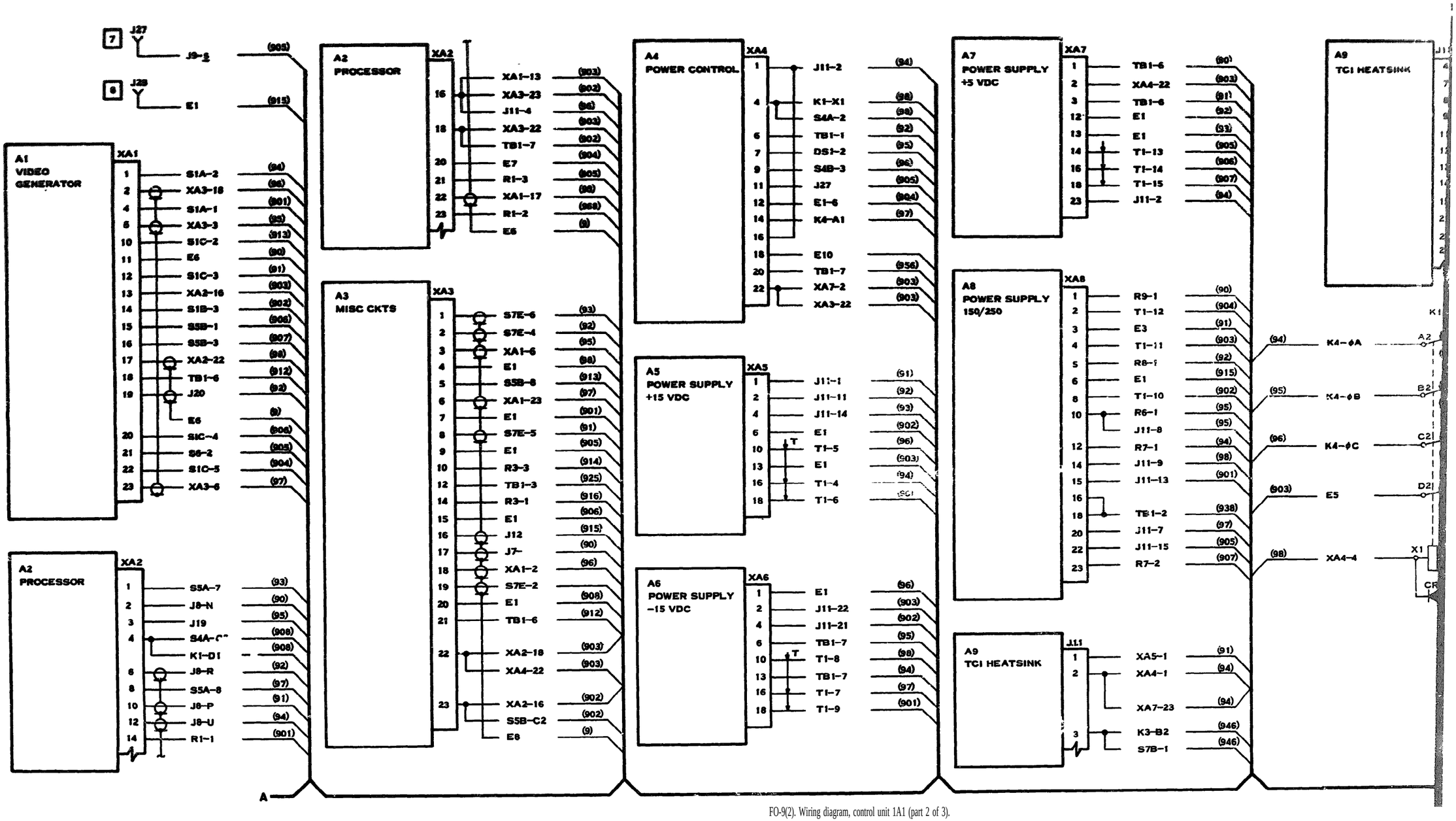


NOTES: UNLESS OTHERWISE SPECIFIED

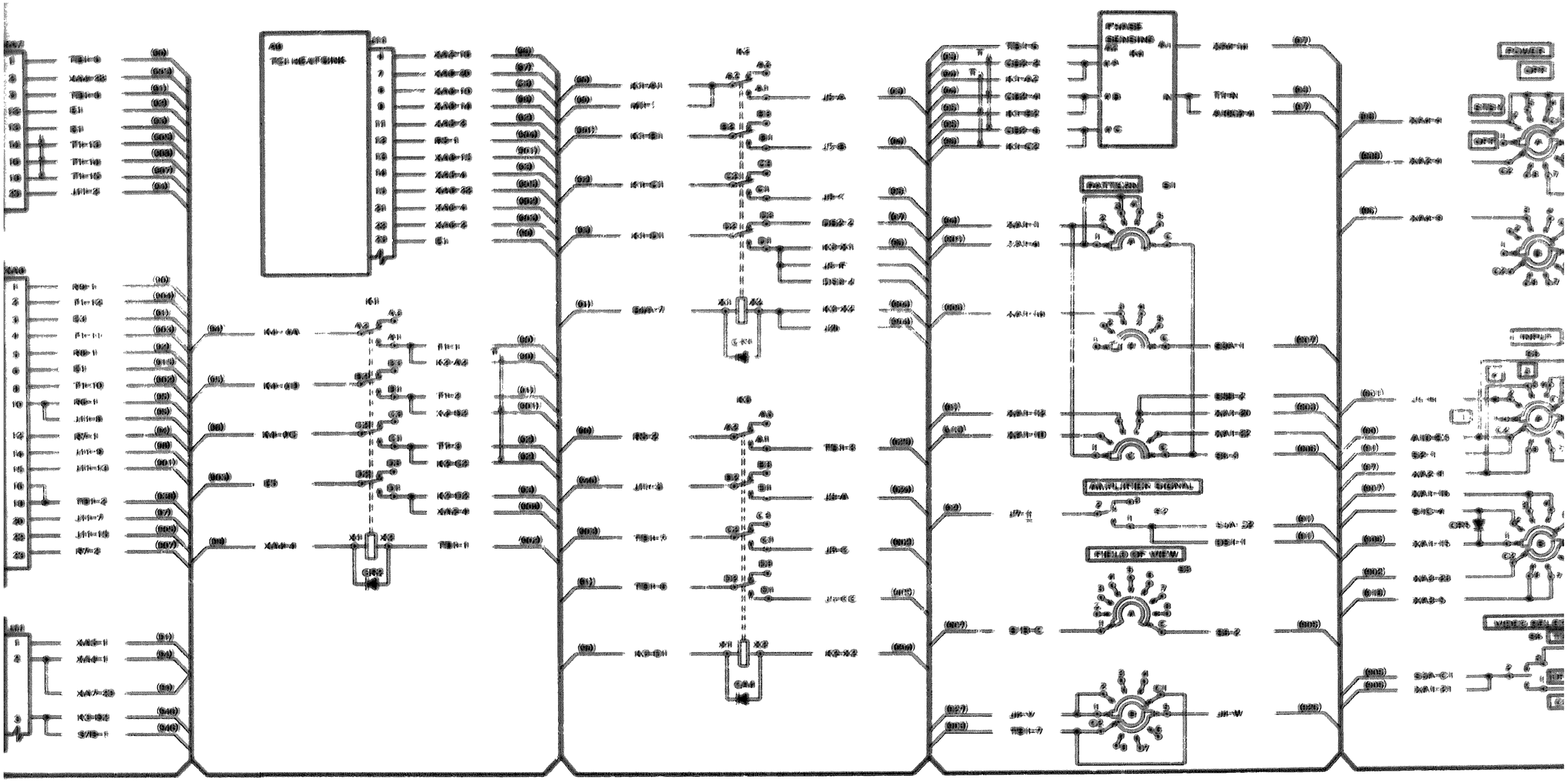
1. ALL WIRES ARE NO. 22 AWG STRANDED.
2. NUMBERS IN PARENTHESIS INDICATE COLOR OF WIRE IN ACCORDANCE WITH USAS STANDARD C83.1.
3. PANEL MARKINGS INDICATED WITHIN RECTANGULAR BOX.
4. FOR COMPLETE REFERENCE DESIGNATION, PREFIX WITH 1A1.

E1.6625-1826-40-TM-12 ①

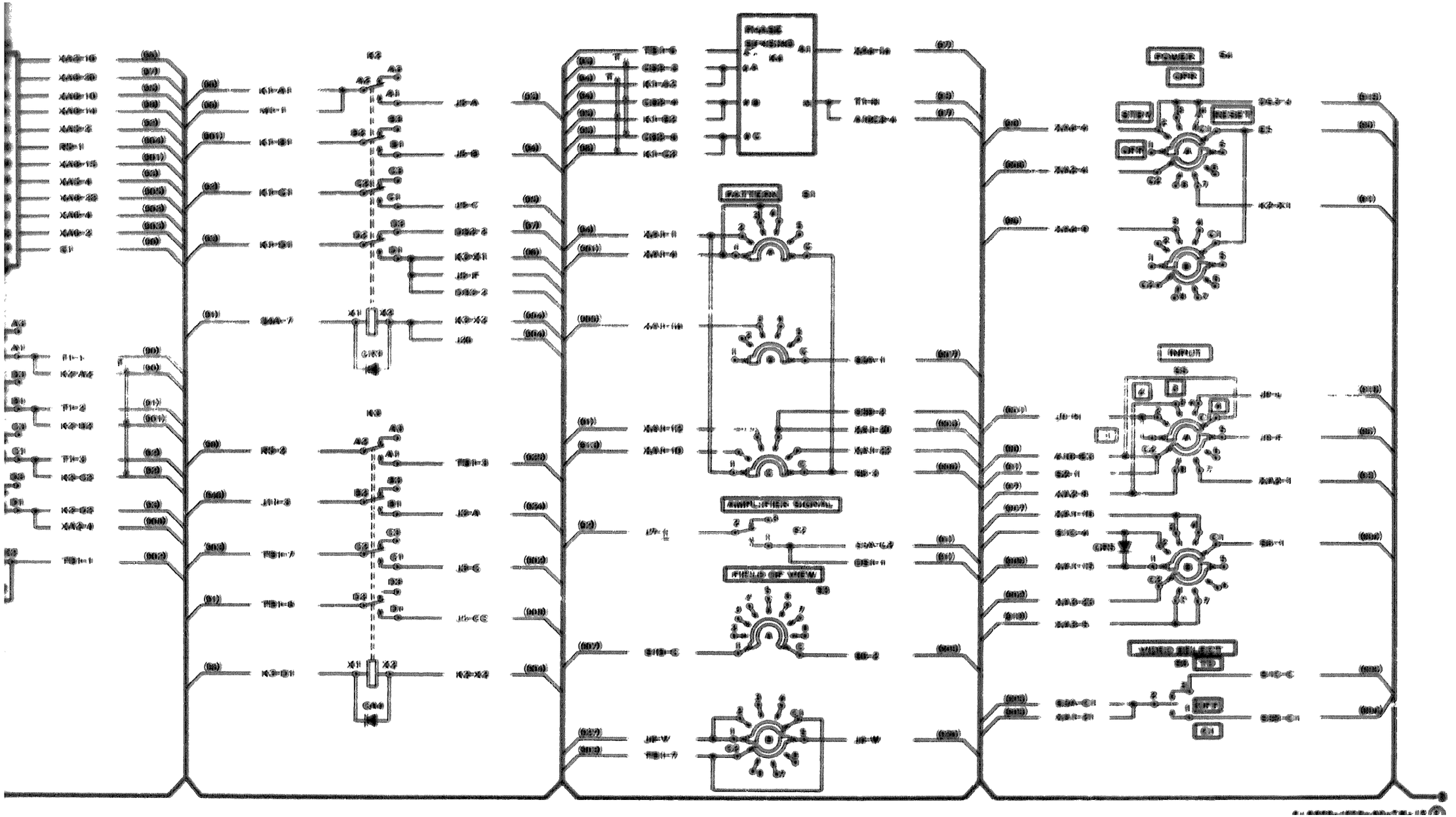
FO-9(1). Wiring diagram, control unit 1A1 (part 1 of 3).



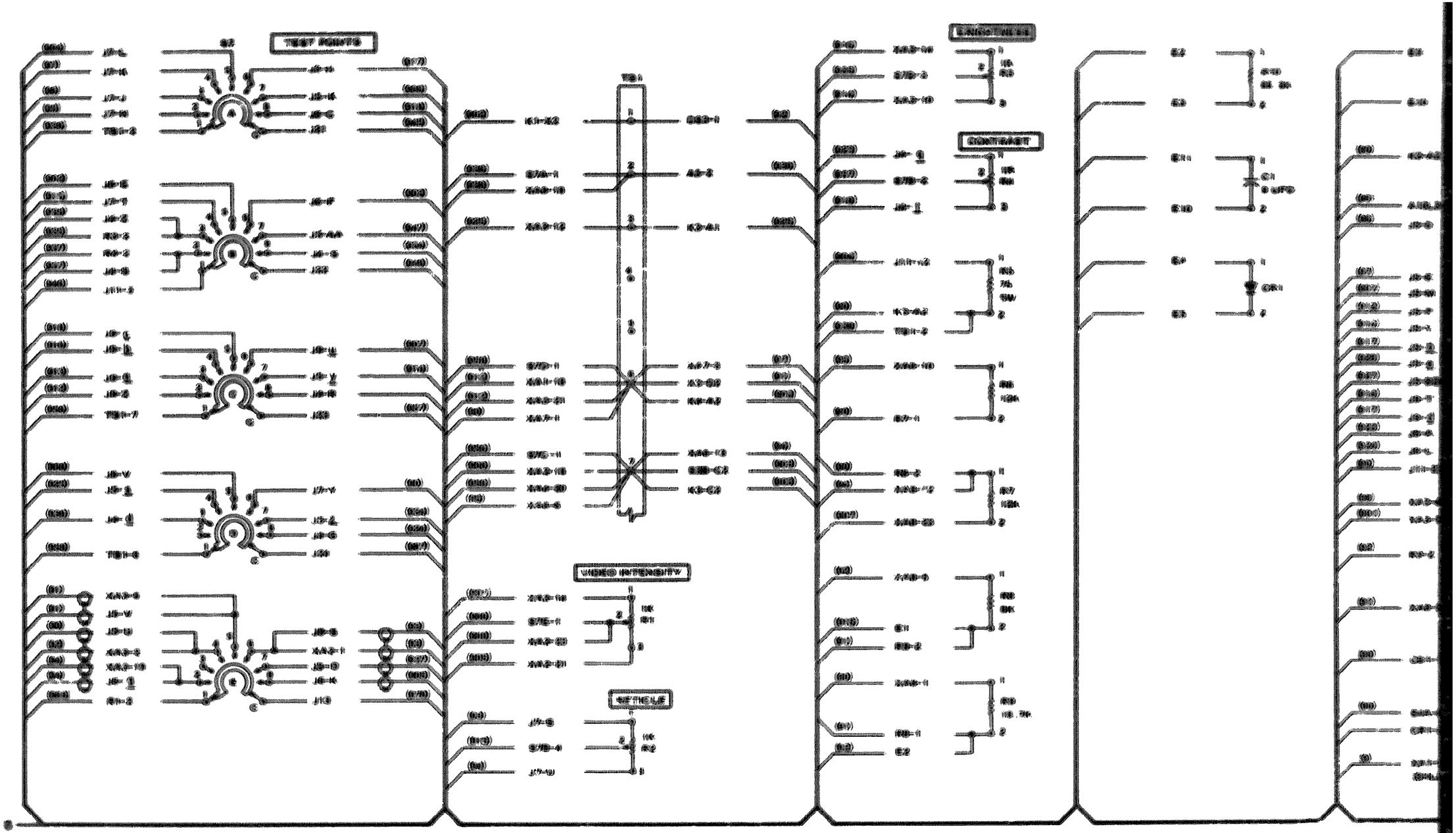
FO-9(2). Wiring diagram, control unit 1A1 (part 2 of 3).



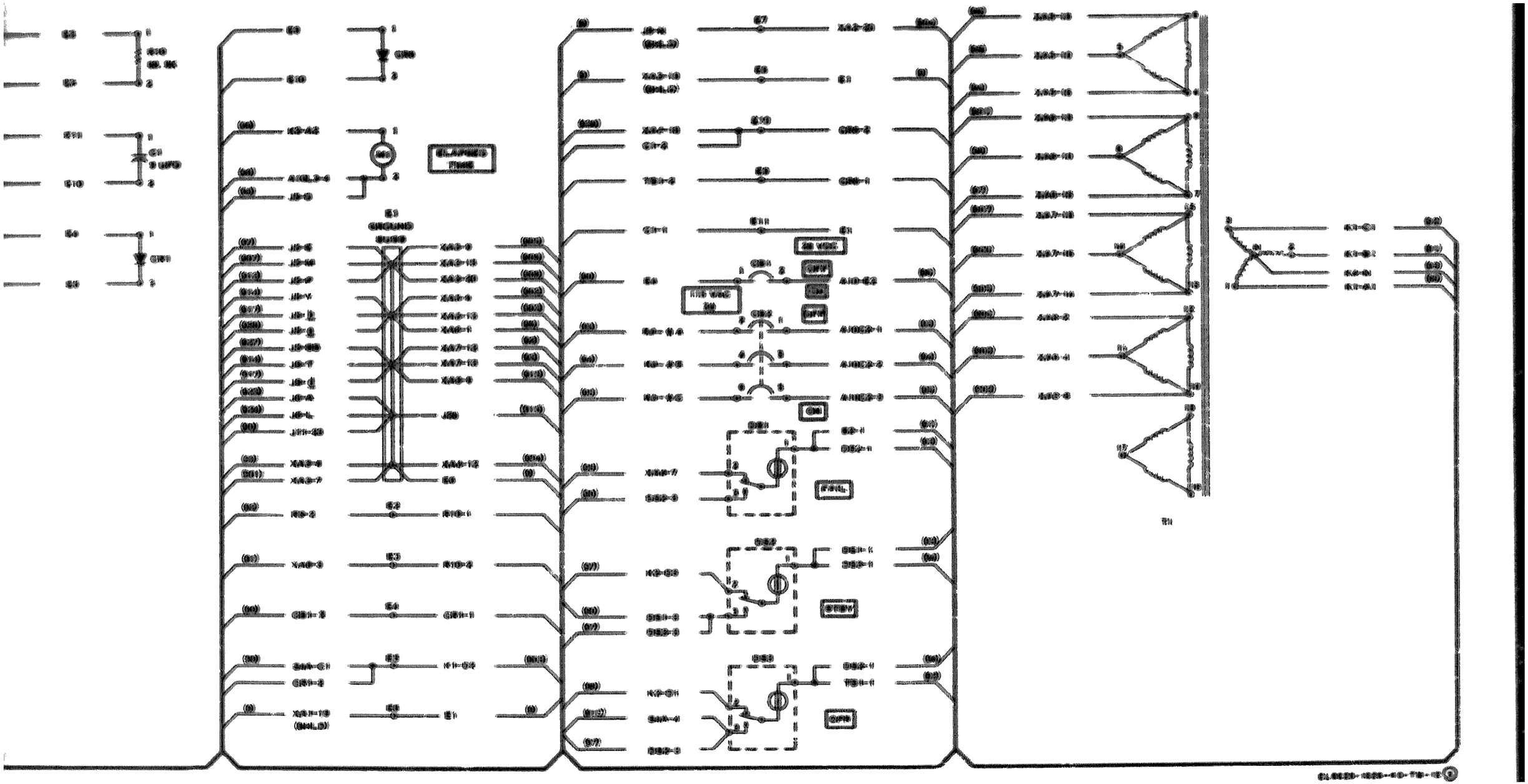
FO-9(3). Wiring diagram, control unit 1A1 (part 3 of 3).



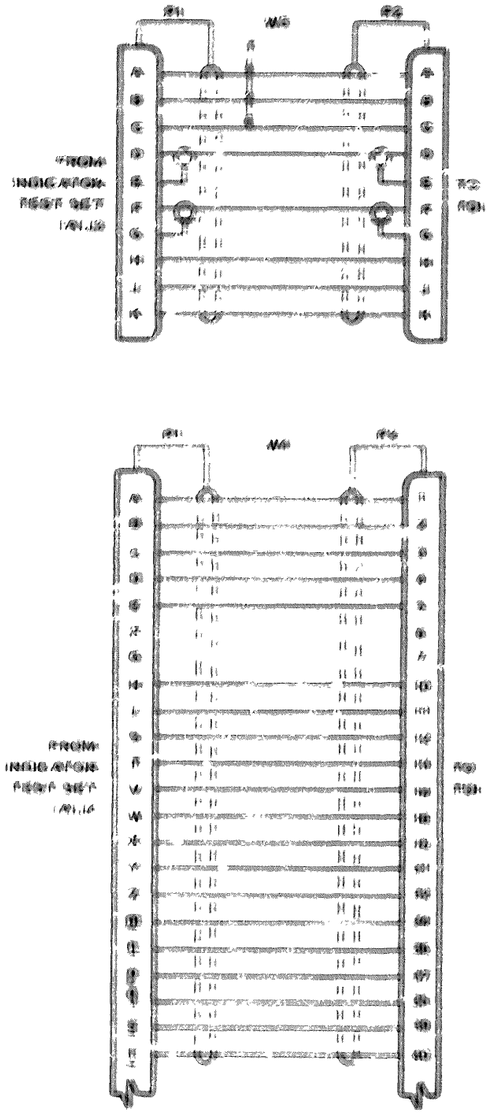
FO-9(3). Wiring diagram, control unit 1A1 (part 3 of 3).

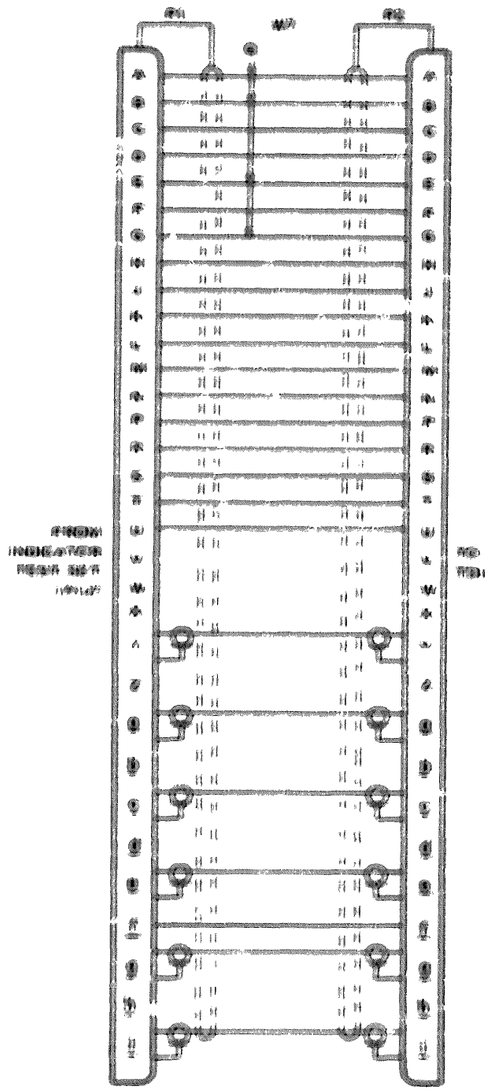


FO-9(8) *Wiring diagram, control unit 1.81 (par*

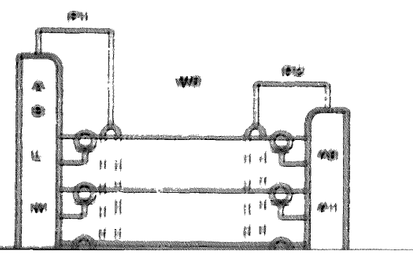


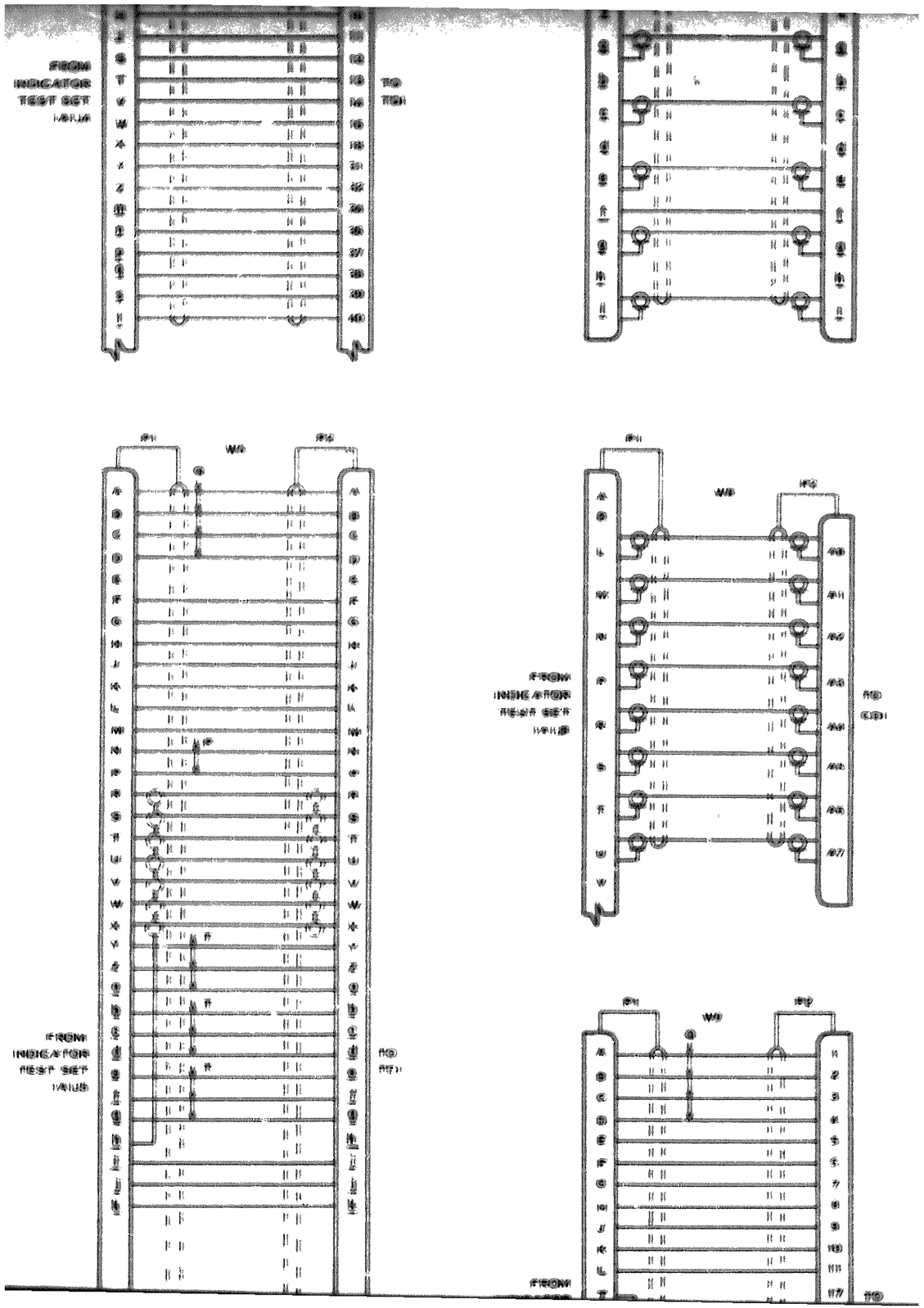
FO-9(3). Wiring diagram, control unit 1A1 (part 3 of 3).

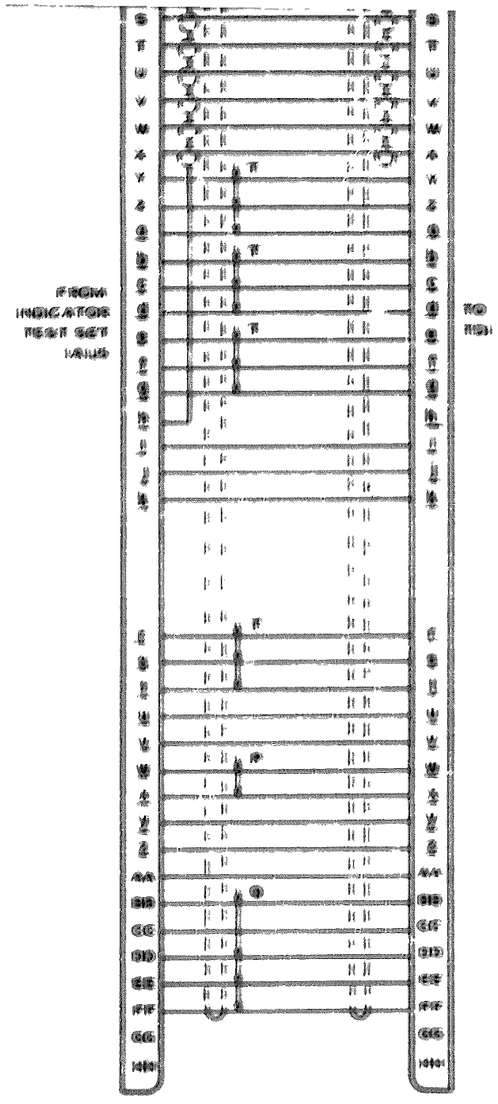

FROM INDICATOR RESET SET (W1,16)
TO RDH

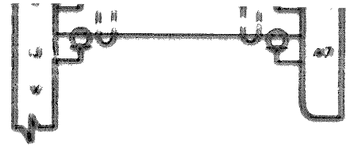

FROM INDICATOR RESET SET (W1,16)
TO RDH

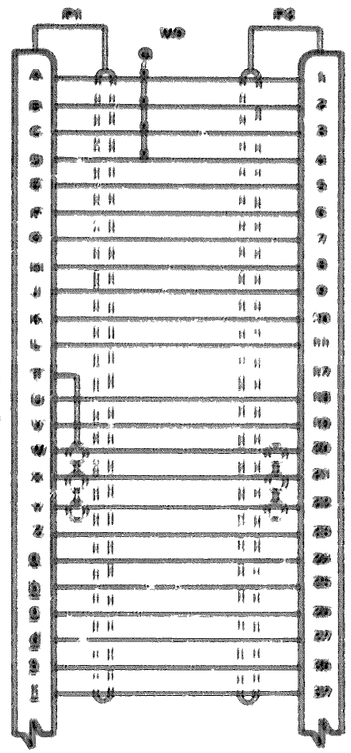
FROM INDICATOR RESET SET (W1,16)
TO RDH

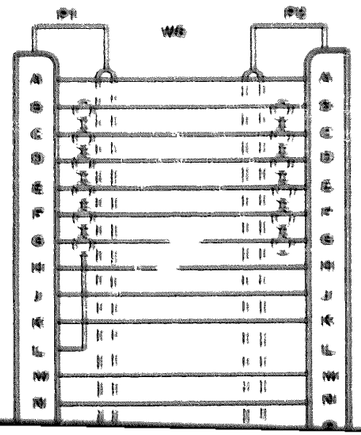


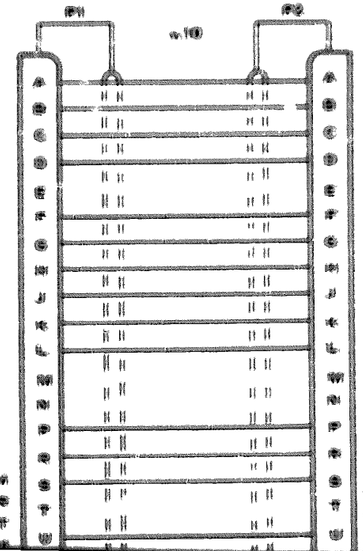

FROM INDICATOR TEST SET
TO TEST
FROM INDICATOR TEST SET
TO TEST
FROM INDICATOR TEST SET
TO TEST
FROM INDICATOR TEST SET
TO TEST

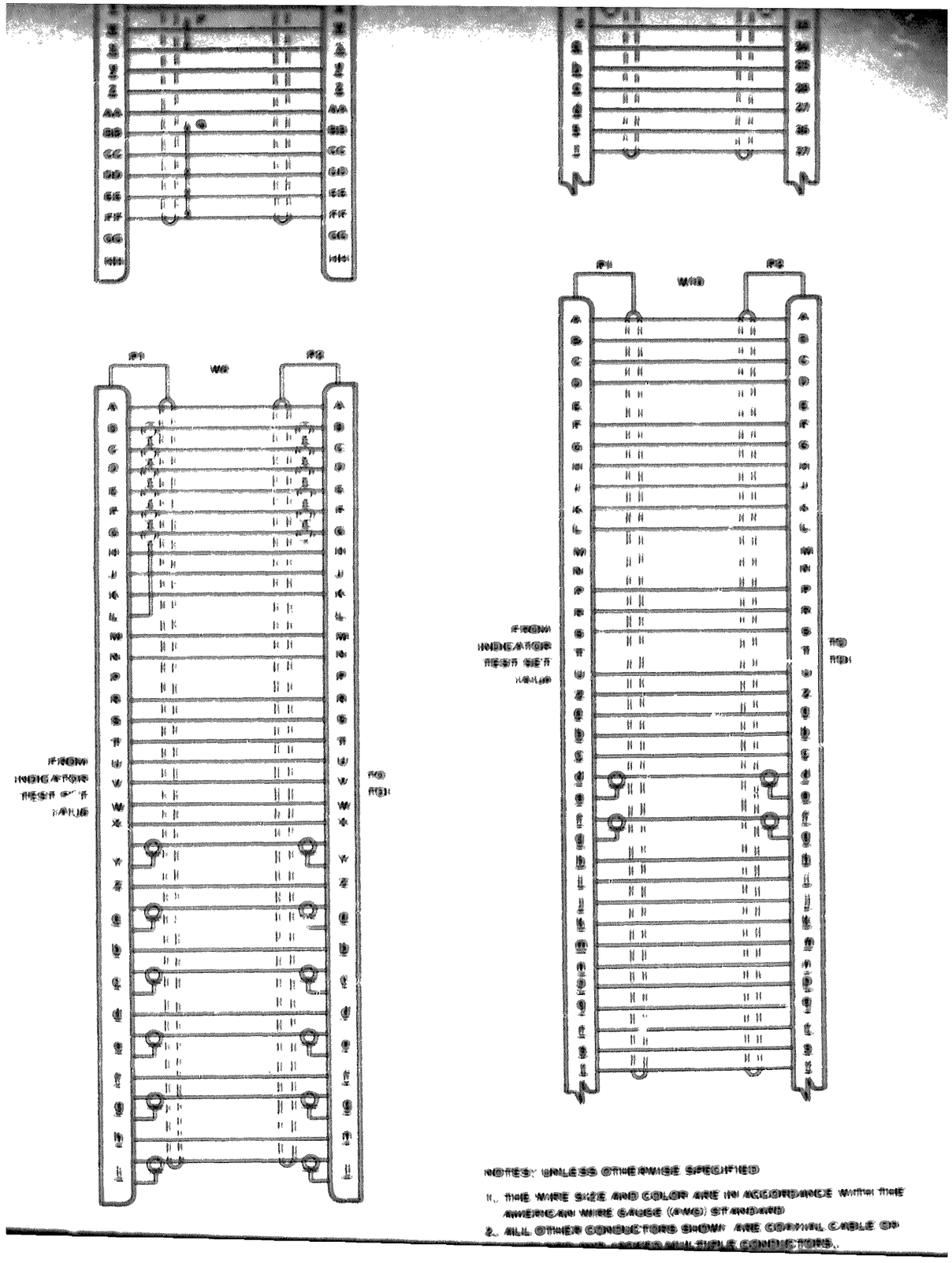

FROM INDICATOR TEST SET
TO TEST SET




P1
W9
P2
FROM INDICATOR TEST SET
TO TEST SET

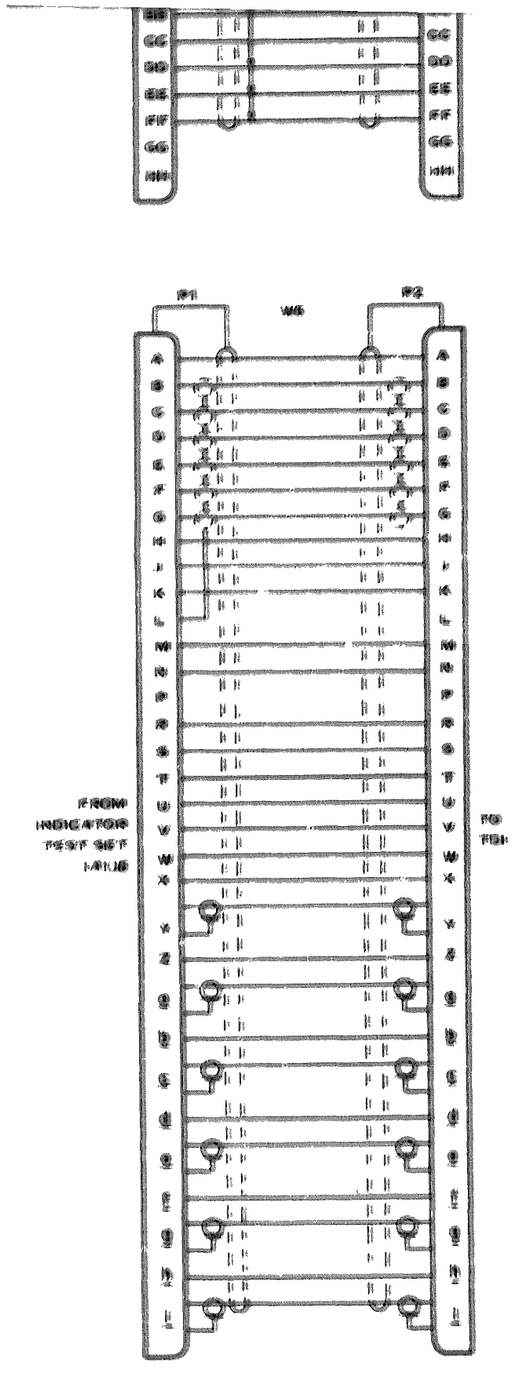

P1
W8
P2

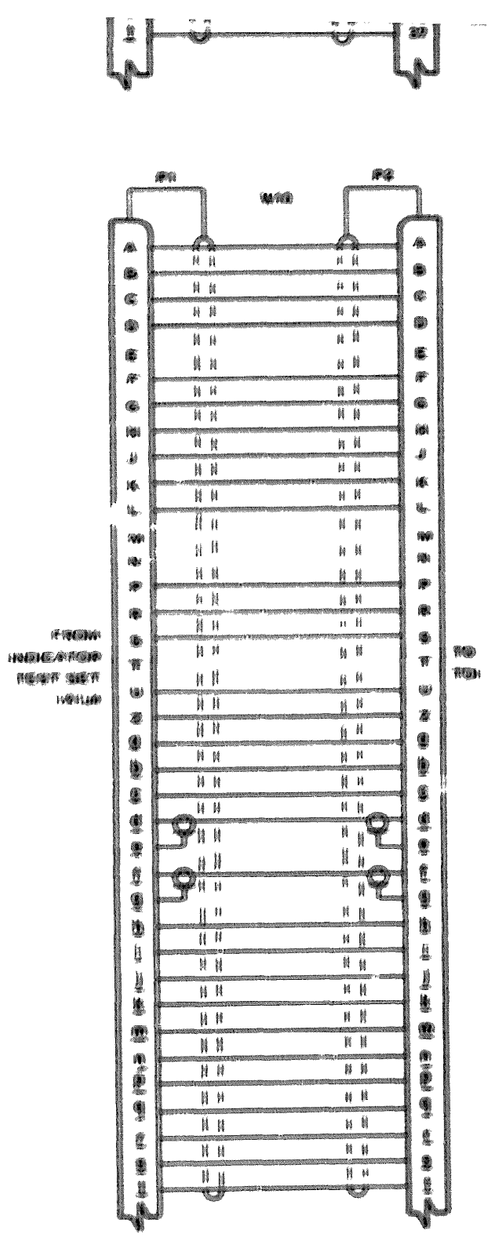

P1
W10
P2
FROM INDICATOR TEST SET
TO TEST SET



NOTES: UNLESS OTHERWISE SPECIFIED

1. THE WIRE SIZE AND COLOR ARE IN ACCORDANCE WITH THE AMERICAN WIRE GAUGE (AWG) STANDARD
2. ALL OTHER CONDUCTORS SHOWN ARE COAXIAL CABLE OR [illegible] MULTIPLE CONDUCTORS.





FO-10.

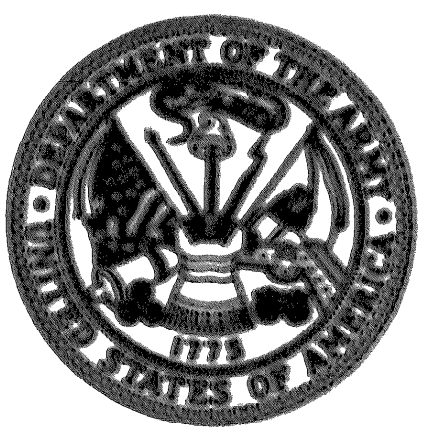
NOTES: UNLESS OTHERWISE SPECIFIED

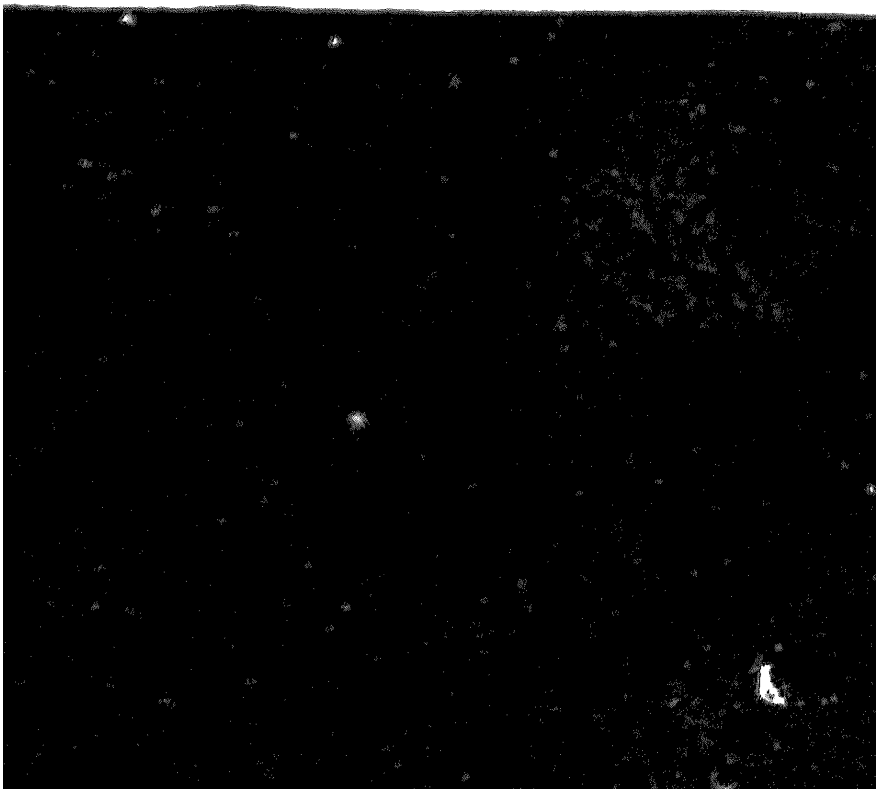
1. THE WIRE SIZE AND COLOR ARE IN ACCORDANCE WITH THE AMERICAN WIRE GAUGE (AWG) STANDARD
2. ALL OTHER CONDUCTORS SHOWN ARE COAXIAL CABLE OR SHIELDED AND TWISTED MULTIPLE CONDUCTORS.
3. ALL WIRES ARE NO. 22 AWG STRANDED.

END

12-25-82

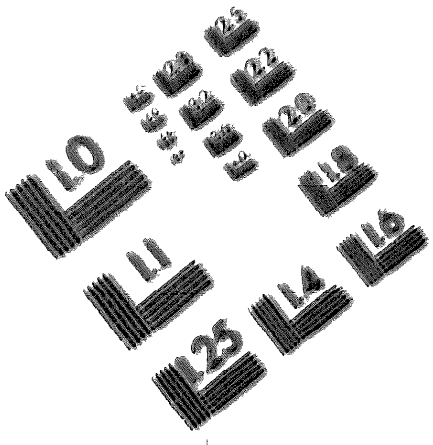
DATE

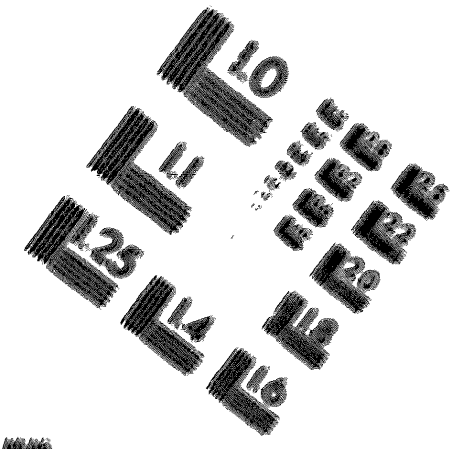




DEPARTMENT OF THE ARMY

MICROFORM
TEST TARGET





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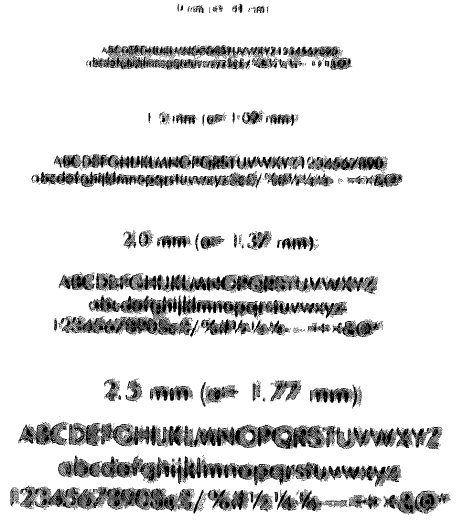
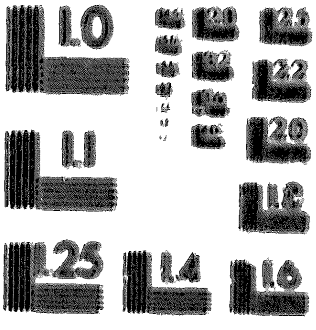
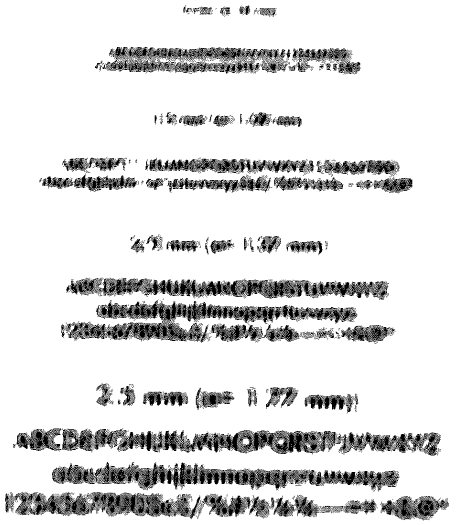
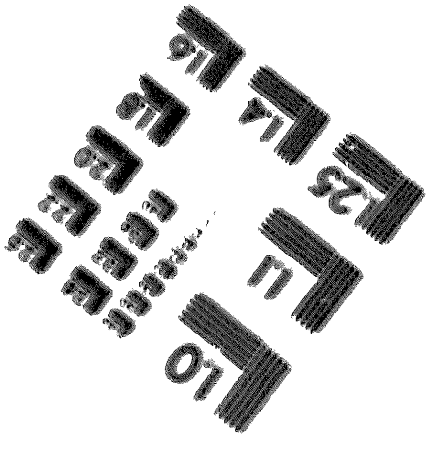
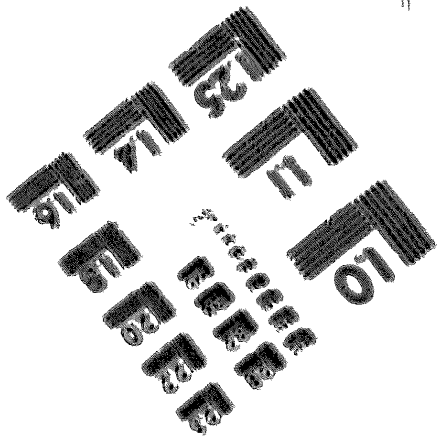






200 MM





230 MM